



C

B

A

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1

LAST\_MODIFIED= Tue Oct 29 15:52:27 2013

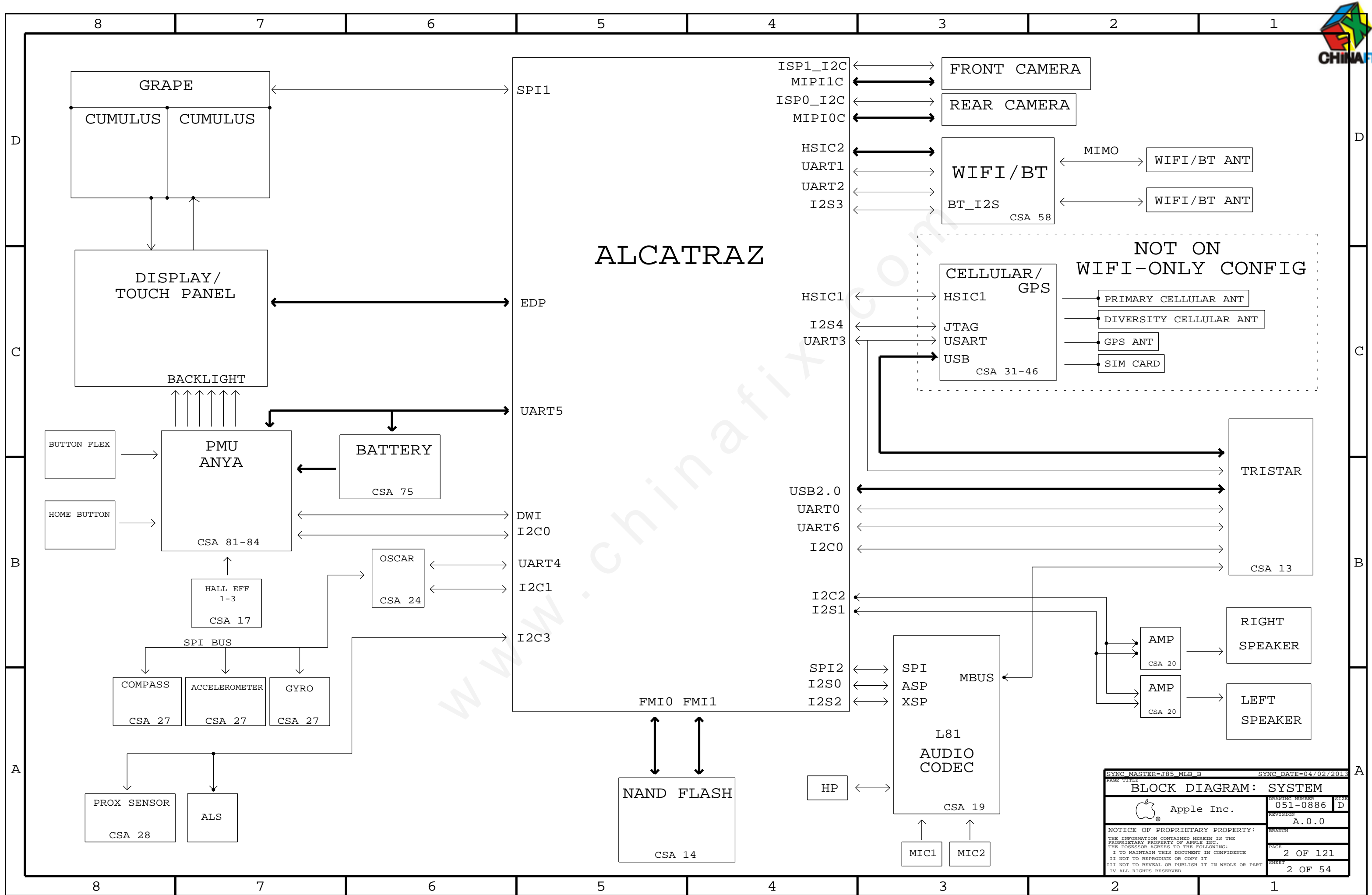
D


2

BA

DRAWING

1



SYNC MASTER=J85 MLB B		SYNC DATE=04/02/2013	
PAGE TITLE			
BLOCK DIAGRAM:		SYSTEM	
 Apple Inc.		DRAWING NUMBER	051-0886
		SIZE	D
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87654321

Page Notes

Power aliases required by this page: (NONE)
Signal aliases required by this page: (NONE)
BOM options provided by this page:

BOM OPTIONS

COMMON  
ALTERNATE  
16GB\_PROD  
32GB\_PROD  
64GB\_PROD  
128GB\_PROD  
DEVELOPMENT\_JTAG\_TAP  
JTAG\_DAP  
MLB (WDOG TO PMU)

WIFI BOM OPTIONS

ANDGATE\_TI  
FERRITE\_TV  
FERRITE\_IDK

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0207	1	H6P + 1GB ELPIDA	U0652	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0208	339S0207		U0652	HYNIX DDR

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0656	1	1C, PMU, ANYA, D2089A1, OTPXX, FCCSP342	U8100	CRITICAL	

FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0921	1	TOS, 19NM, PPN1.5, C, DDP, 16GB	U1400	16GB
335S0922	1	TOS, 19NM, PPN1.5, C, QDP, 32GB	U1400	32GB
335S0923	1	TOS, 19NM, PPN1.5, C, ODP, 64GB	U1400	64GB
335S0929	1	TOS, 19NM, PPN1.5, C, 12DP, 64GB	U1400	96GB
335S0924	1	TOS, 19NM, PPN1.5, C, 16DP, 128GB	U1400	128GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0930	335S0921	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0931	335S0922	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0932	335S0923	64GB	U1400	HYNIX 20NM PPN1.5 64GB

U2200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4272	1	1C, SIGMA142IV, PMU, SW, GREENFET3, AA, TQFN	U2200	

NOTE: FOLLOWING J72, U2200 USES 353S3672 FOOTPRINT (353S4272 HAS SMALLER PADS DUE TO NEW DFM RULES)

4.3UF CAP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		C1009, C1015...	RDAR #13988471

WIFI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0223	339S0213		U5800	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-6207	1	FENCE, TALL, MLB, X221	PD_FENCE_MLB	CRITICAL	
806-7613	1	FENCE, RADIO, MLB, C BRD, X221	PD_CAN_RADIO	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-5393 (X200C1 GOOD)	FNJD	CRITICAL	EEEE_X200C_GOOD
825-7639	1	EEEE FOR 639-5394 (X200C1 BETTER)	FNJ5	CRITICAL	EEEE_X200C_BETTER
825-7639	1	EEEE FOR 639-5385 (X200C1 BEST)	FNJ9	CRITICAL	EEEE_X200C_BEST
825-7639	1	EEEE FOR 639-5386 (X200C1 BEST+)	FNJH	CRITICAL	EEEE_X200C_BEST+
825-7639	1	EEEE FOR 639-5387 (X200C1 ULTIMATE)	FNJ6	CRITICAL	EEEE_X200C_ULTIMATE
825-7639	1	EEEE FOR 639-5388 (X200C1 GOOD IVS)	FNJ8	CRITICAL	EEEE_X200C_GOOD_IVS
825-7639	1	EEEE FOR 639-5389 (X200C1 BETTER IVS)	FNJF	CRITICAL	EEEE_X200C_BETTER_IVS
825-7639	1	EEEE FOR 639-5390 (X200C1 BEST IVS)	FNJC	CRITICAL	EEEE_X200C_BEST_IVS
825-7639	1	EEEE FOR 639-5391 (X200C1 BEST+ IVS)	FNJ7	CRITICAL	EEEE_X200C_BEST+_IVS
825-7639	1	EEEE FOR 639-5392 (X200C1 ULTIMATE IVS)	FNJG	CRITICAL	EEEE_X200C_ULTIMATE_IVS

GYRO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1192	1	GYRO, ST MICRO	U2720	CRITICAL	GYRO_STMICRO
338S1218	1	GYRO, INVENSENSE	U2720	CRITICAL	GYRO_INVENSENSE
132S0391	1	CAP 0.01UF 25V 0201	C2726	CRITICAL	GYRO_STMICRO
132S0288	1	CAP 0.1UF 16V 0201	C2726	CRITICAL	GYRO_INVENSENSE

338S1158 OLD GYRO - ST MICRO  
OLDER INVENSENSE P/N 338S1135  
OLD INVENSENSE P/N 338S1200 (3/22/13)


ACCEL

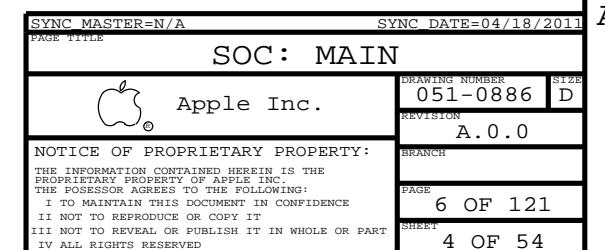
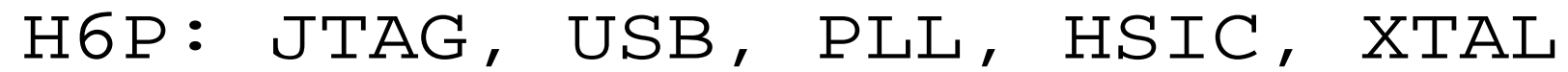
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1163	1	1C, ACCEL, 3-AXIS, DIG, BMA282, LGA14	U2700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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338S1233 ST MICRO - DISQUAL'ED  
338S1114 OLD ACCEL - ST MICRO  
338S1191 OLD ACCEL - ST MICRO

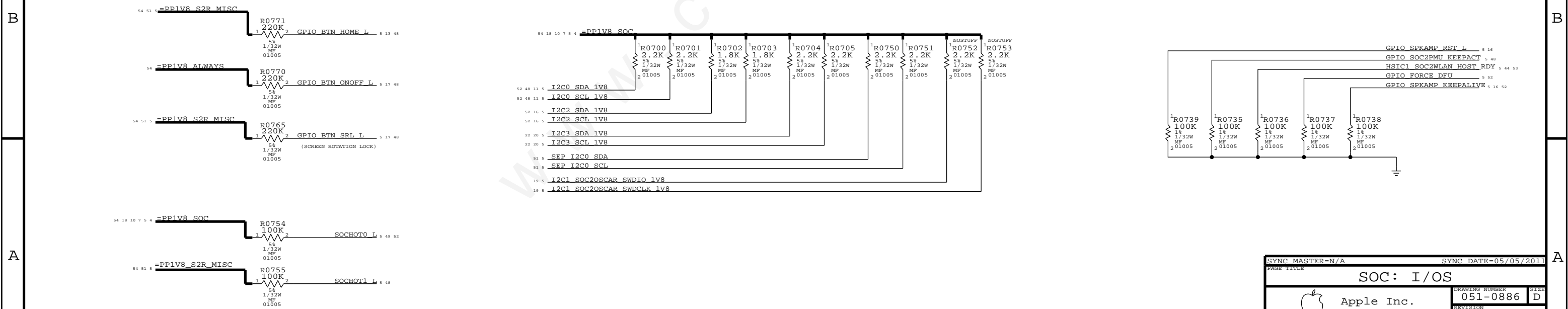
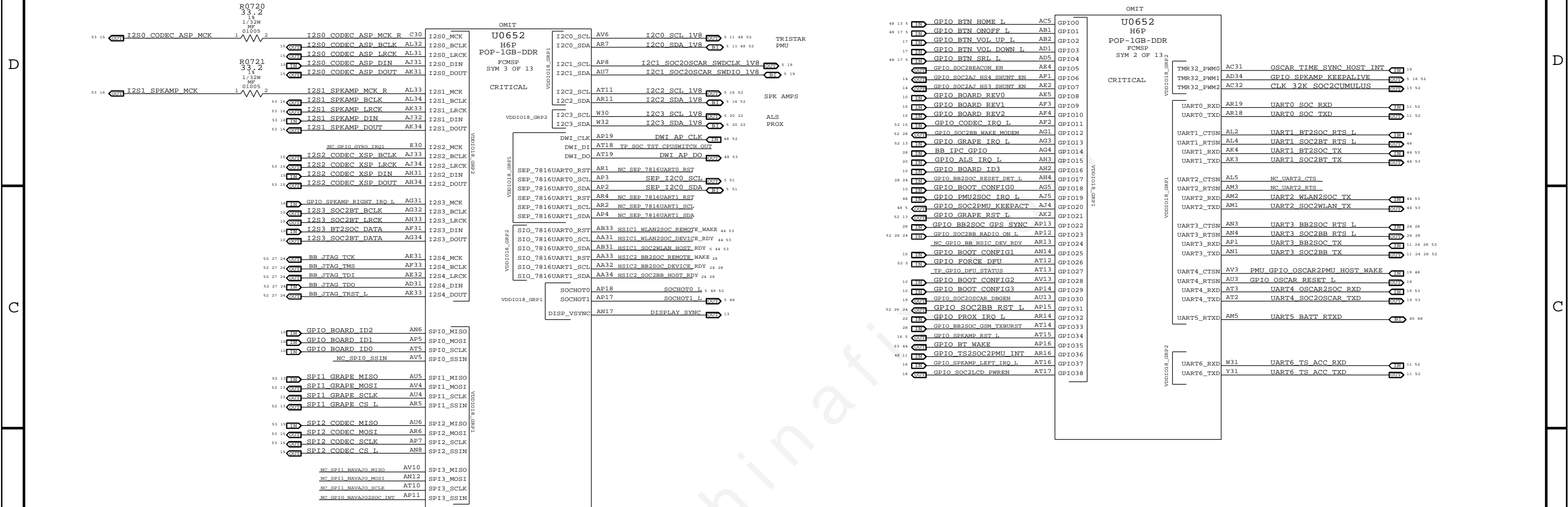
SYNC MASTER=J72 MLB C SYNC DATE=11/26/2012

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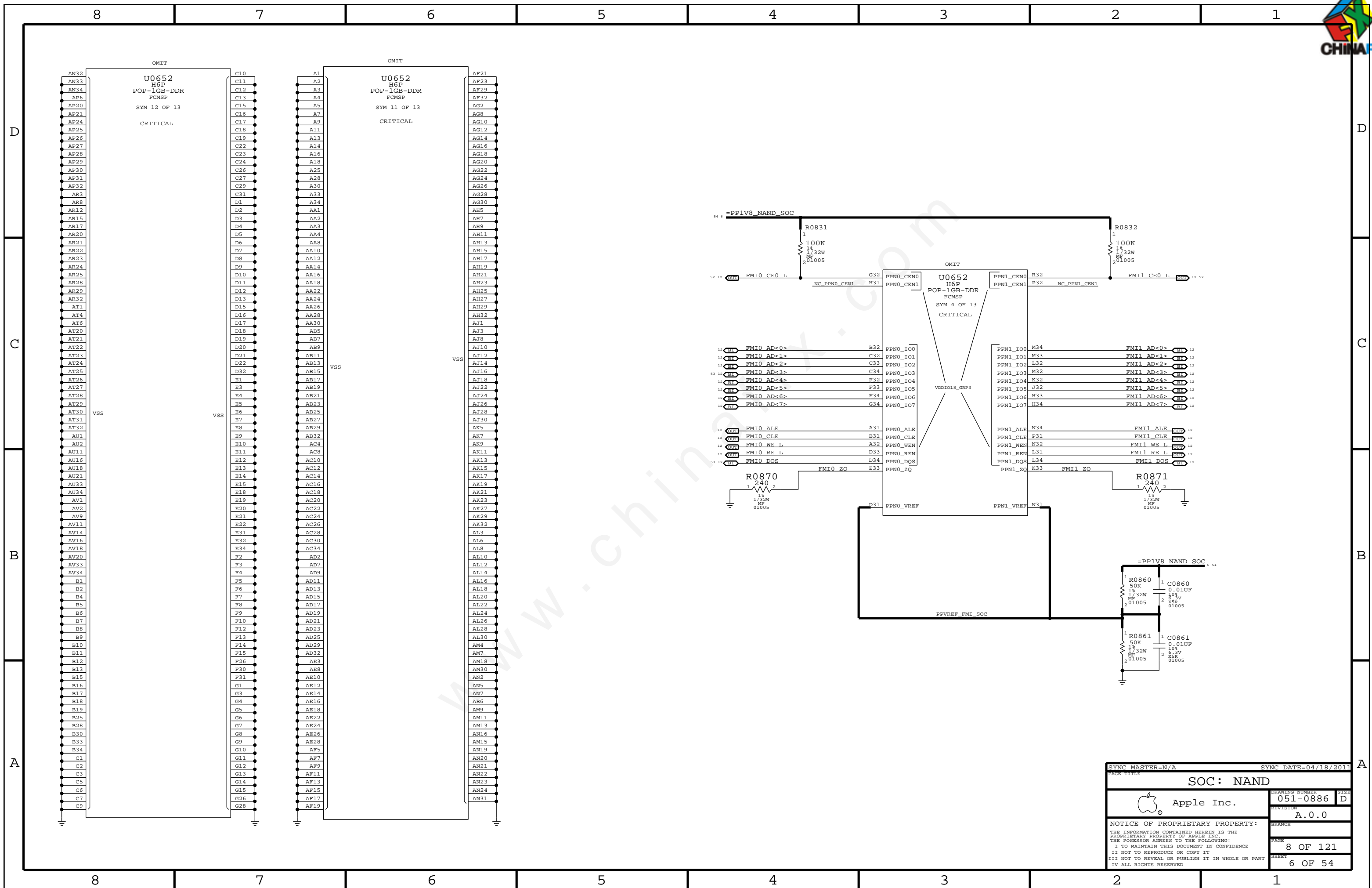




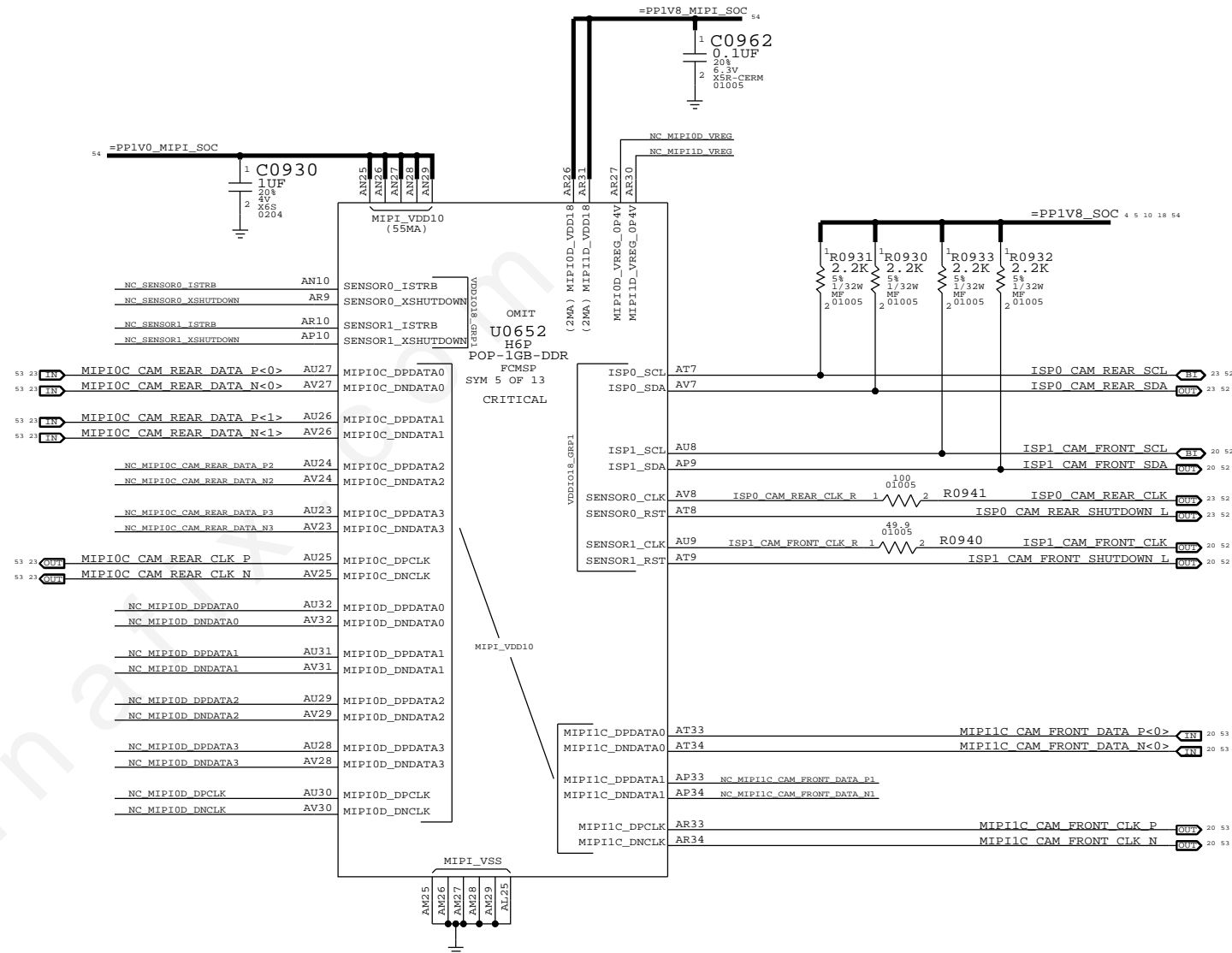
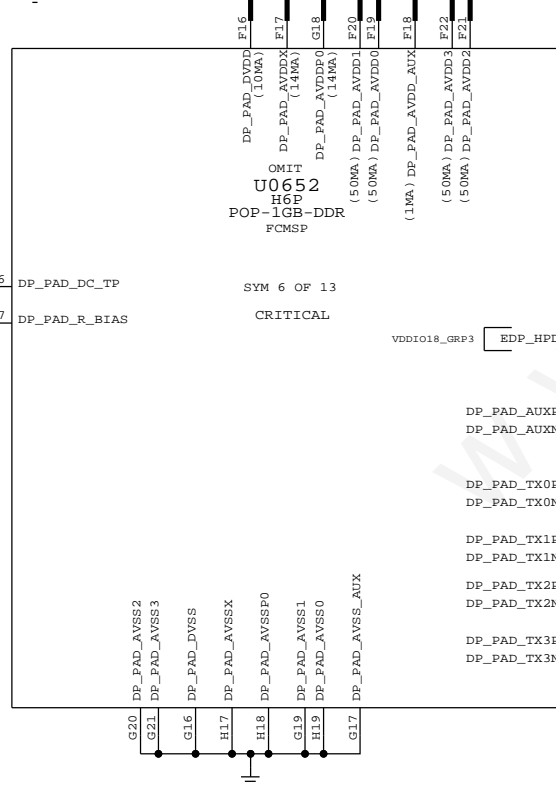
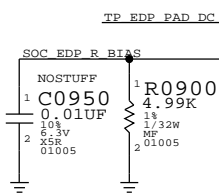
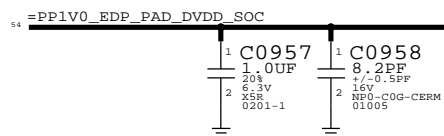
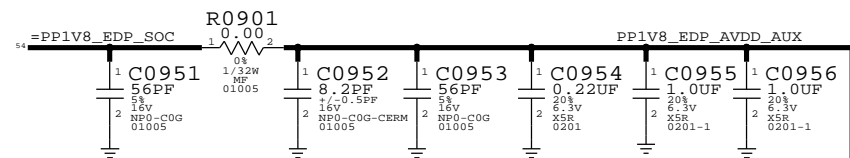
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
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Apple Inc.		051-0886	
REVISION		SIZE	
A.0.0		D	
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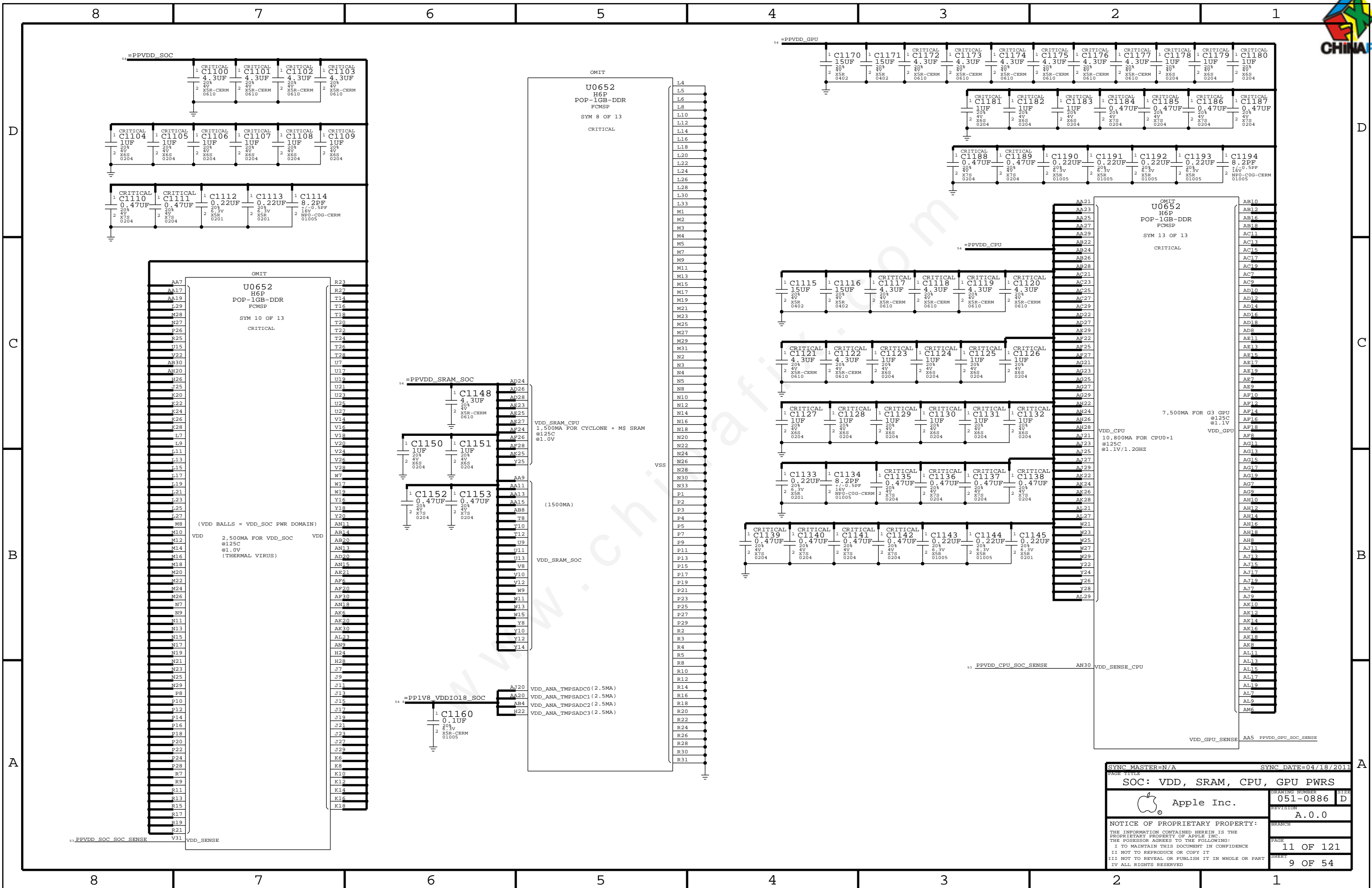


## DISPLAYPORT



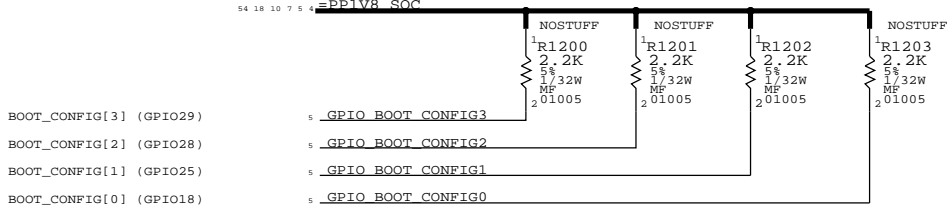


SYNC MASTER=N/A		SYNC DATE=04/18/2011	
PAGE TITLE			
SOC: SRAM, IO PWSR			
 Apple Inc.	GRANTING NUMBER	SIZE	
	051-0886	D	
	REVISION	A.0.0	
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SHEET	8 OF 54		



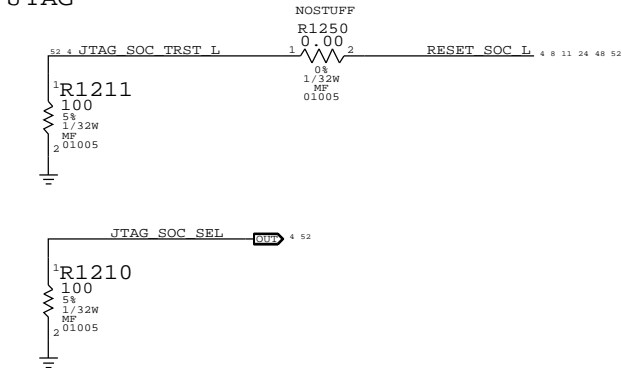


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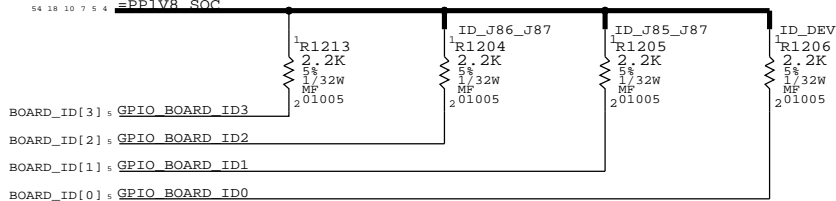


BOOT_CONFIG[3-0]		S/W READ FLOW
0000	SPI0	1. SET GPIO AS INPUT
0001	SPI0 TEST MODE	2. DISABLE PU AND ENABLE PD
0010	NAND	3. READ
0011	NAND TEST MODE	

# JTAG

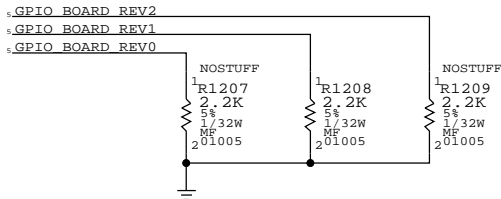


# BOARD ID



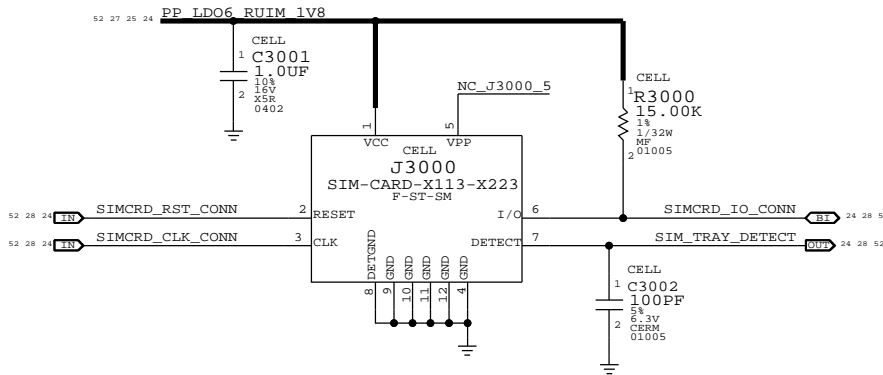
ID[3-0]	SYSTEM	S/W READ FLOW
1010	J85 AP	1. SET GPIO AS INPUT
1011	J85 DEV	2. DISABLE PU AND ENABLE PD
1100	J86 AP	3. READ
1101	J86 DEV	
1110	J87 AP	
1111	J87 DEV	

# BOARD REVISION



BRD_REV[2-0]	S/W READ FLOW
101	1. SET GPIO AS INPUT
	2. ENABLE PU AND DISABLE PD
	3. READ

# SIM CARD

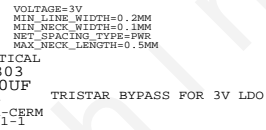



CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

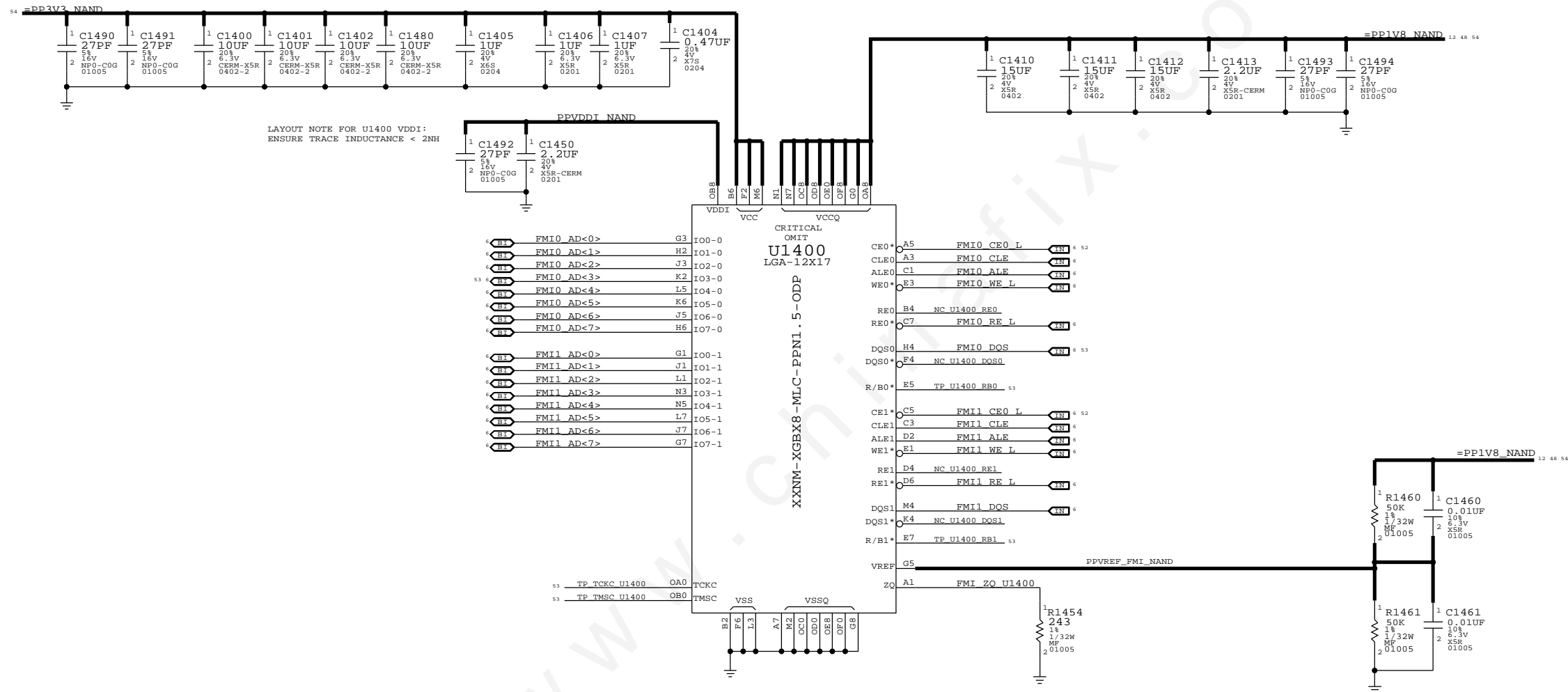
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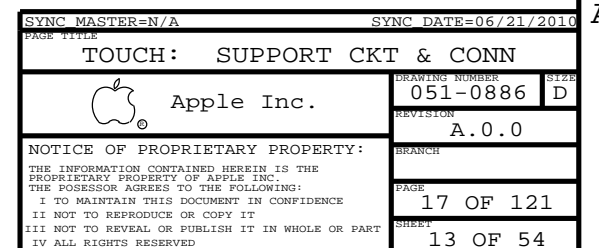
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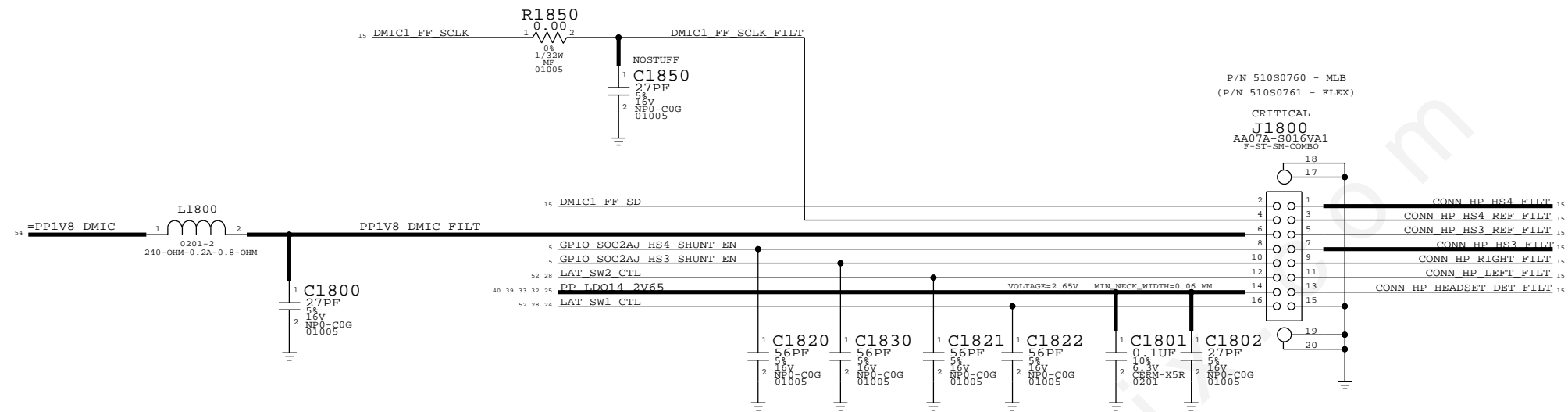


SYMC MASTER-N/A		SYMC DATE-N/A	
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	Apple Inc.		DRAWING NUMBER <b>051-0886</b>
			SIZE <b>D</b>
		REVISION <b>A.0.0</b>	
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SYNC MASTER=MLB		SYNC DATE=05/04/2012	
PAGE TITLE			
NAND STORAGE			
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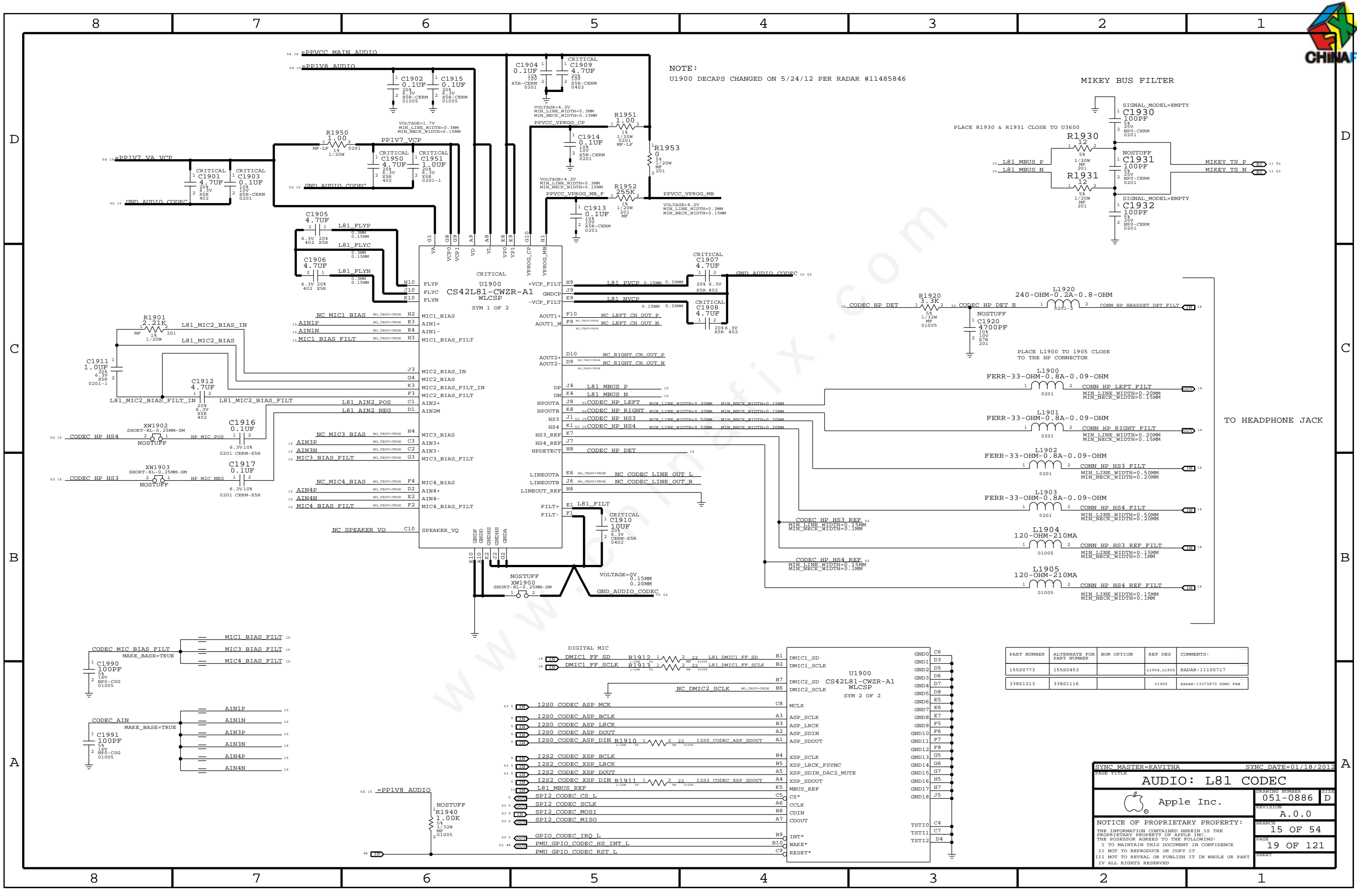




AUDIO\_JACK\_FLEX RET2  
AUDIO\_JACK\_FLEX MIC1  
AUDIO\_JACK\_FLEX MIC2  
AUDIO\_JACK\_FLEX RET1

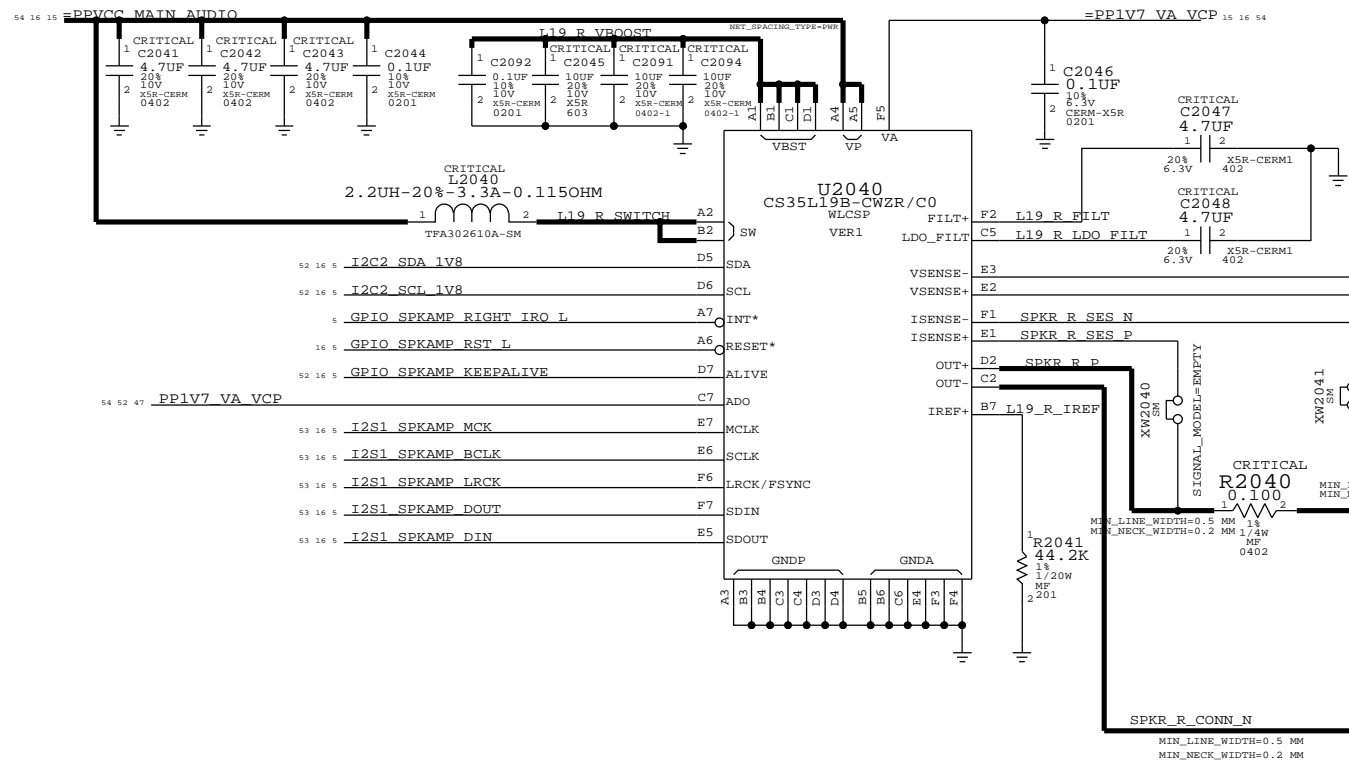
PER DAVE BREECE

SYNC MASTER=N/A		SYNC DATE=03/31/2011	
PAGE TITLE			
AUDIO: HP FLEX CONN			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-0886		D
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	BRANCH		14 OF 54
	PAGE		18 OF 121
	SHEET		



# RIGHT SPEAKER AMP

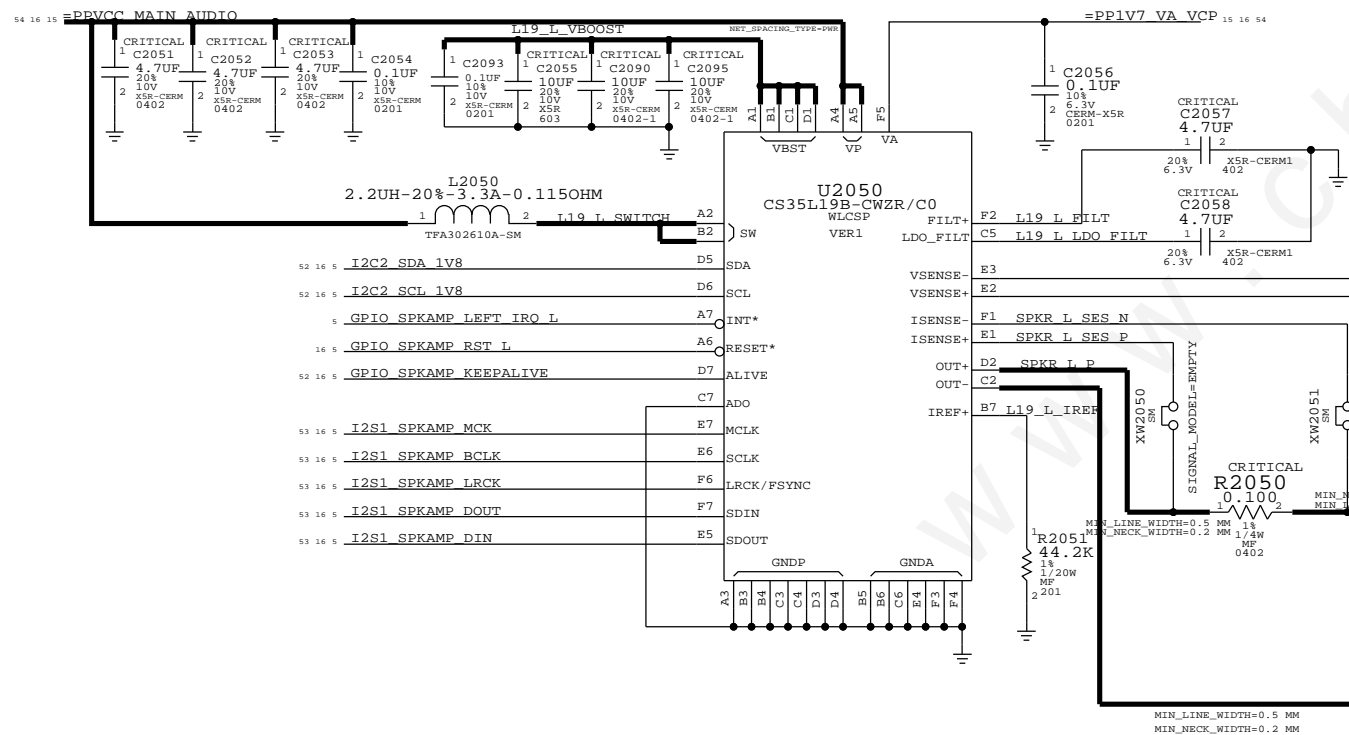
I2C ADDRESS: 1000001X



# SPEAKER CONNECTOR


# LEFT SPEAKER AMP

I2C ADDRESS: 1000000X



# UPDATED: DEC 13

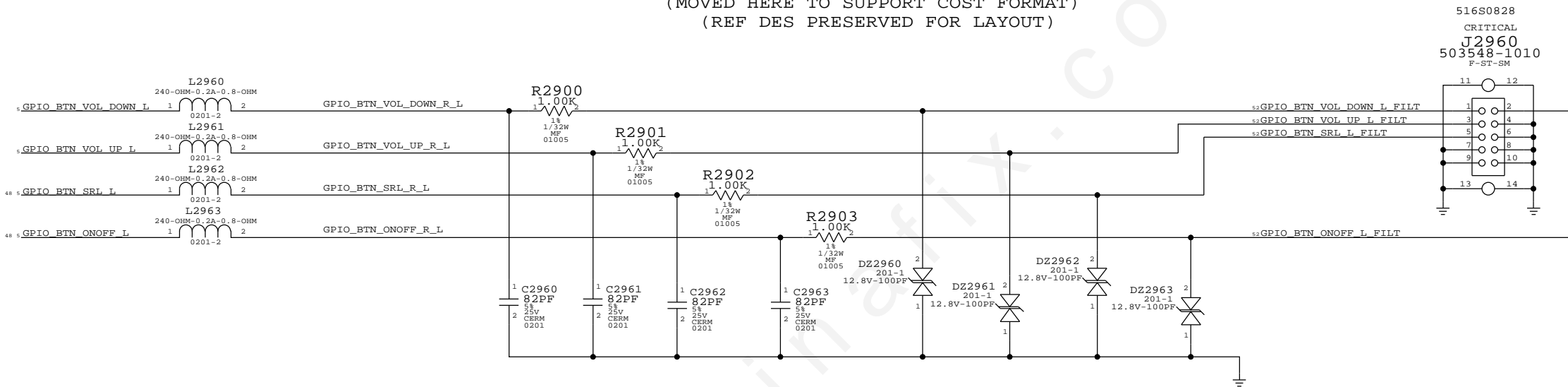
1. ALL THE EMI/DESENSE FILTER COMPONENTS HAVE BEEN REMOVED BASED ON PERFORMANCE ON J65
2. THE CURRENT VERSION OF L19 IS B0 AND WILL CHANGE TO C0 BY MARCH 2013. C0 FIXES PROCESS ISSUES.


SYNC MASTER=KAVITHA		SYNC DATE=01/18/2012	
PAGE TITLE			
AUDIO: CS35L19A AMPS			
 Apple Inc.		DRAWING NUMBER	051-0886
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# BUTTON CONNECTOR

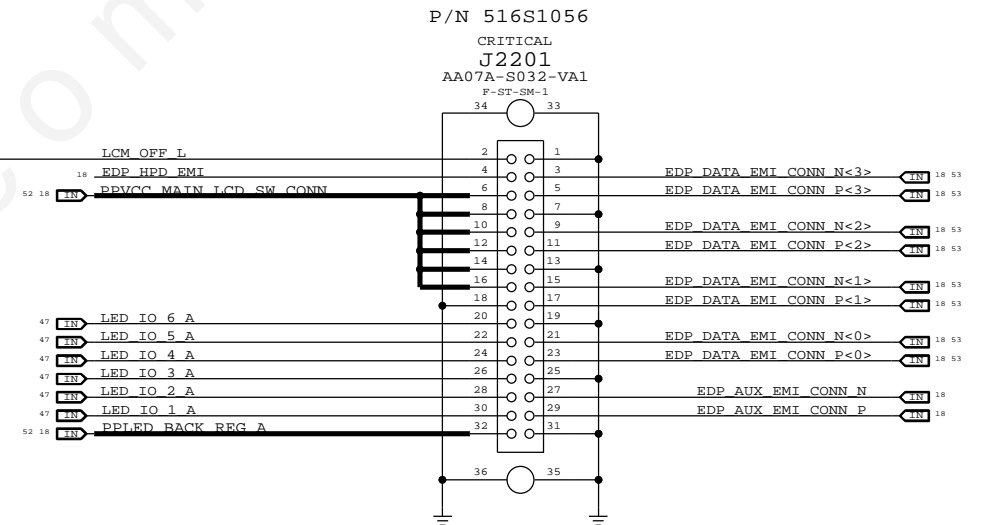
(MOVED HERE TO SUPPORT COST FORMAT)  
 (REF DES PRESERVED FOR LAYOUT)




SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
BUTTON: CONN			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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[illegible]

LAYOUT NOTE:  
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION

[illegible]

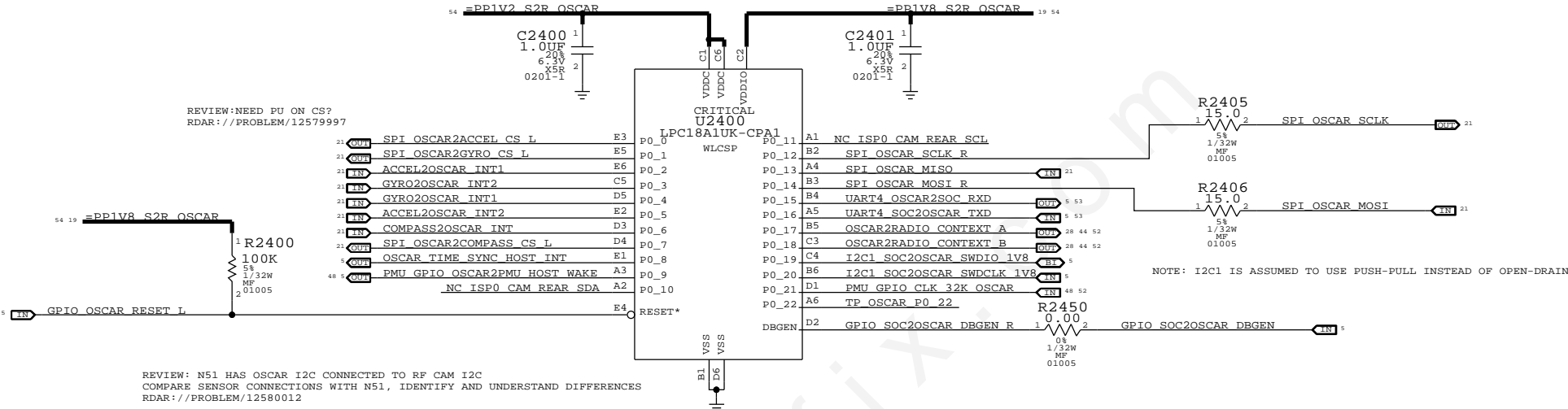
The schematic diagram illustrates the power supply section of the L2240. It features a 240-ohm, 25W resistor (L2240) connected to a 20.0K resistor (R2250) and a 20.0K resistor (R2242). The circuit is powered by a 16V source (C2260) and includes a 1/32W resistor (R2242). The components are labeled with their respective values and part numbers, and the circuit is shown with various electrical symbols and connections.

SYMC MASTER-J85 MLB C		SYMC DATE=12/05/2012	
PAGE TITLE		PAGE NO.	
VIDEO: EDP SUPPORT & CONN			
 Apple Inc.		DRAWING NUMBER	051-0886
		SIZE	D
		REVISION	A.0.0
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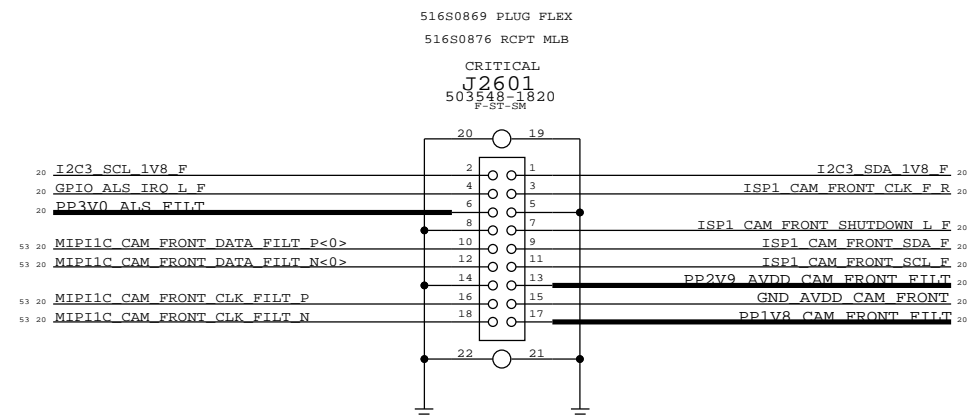
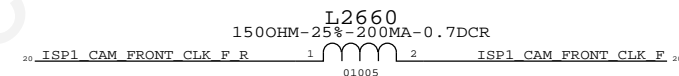
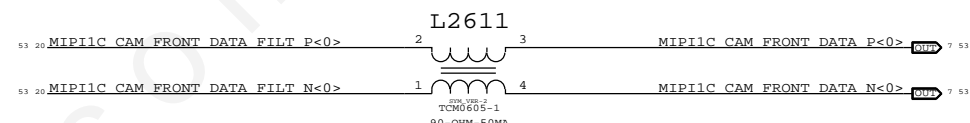
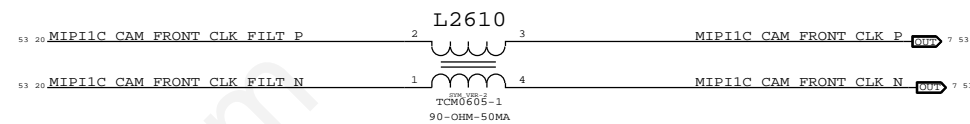
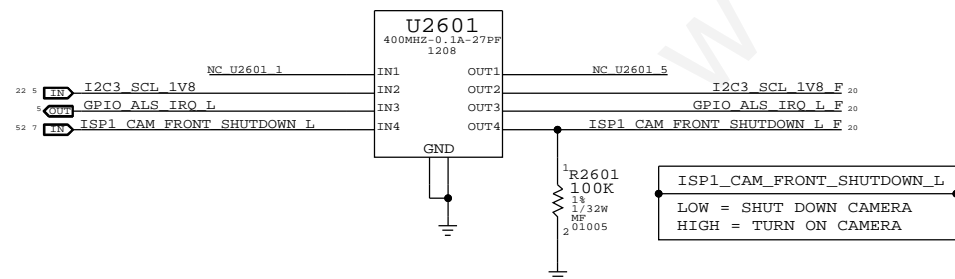
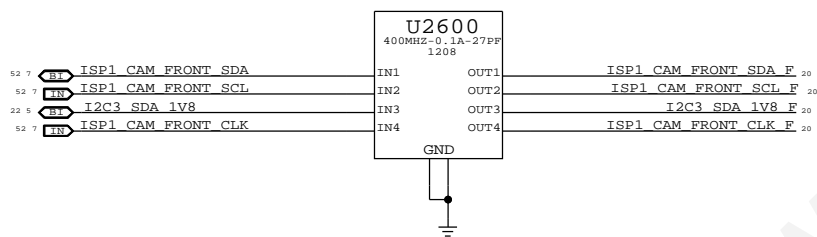
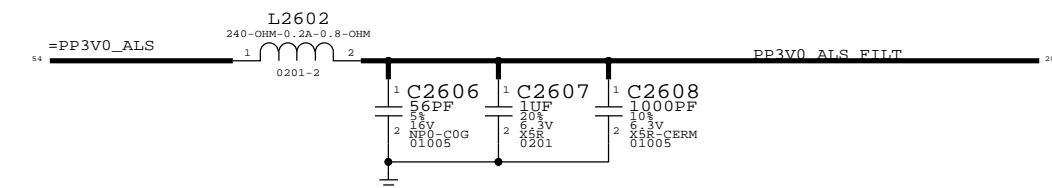
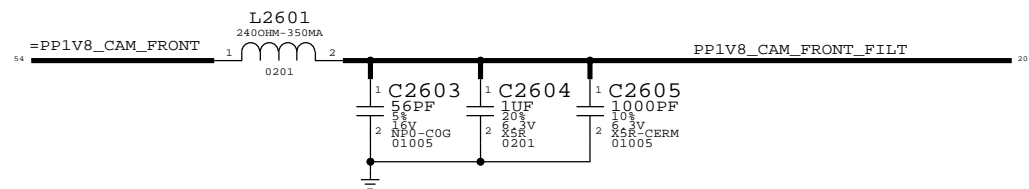
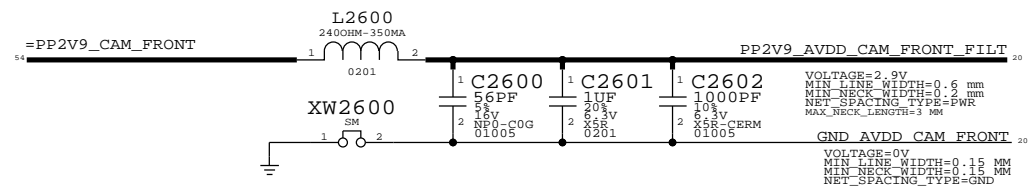
OSCAR

APN 337S4416

OSCAR VDDIO = 1.8V HIBERNATE (NEED TO WAKE HOST)  
OSCAR CORE = 1.2V HIBERNATE (NEED TO RUN IN S2R)



## VGA FRONT CAMERA CONNECTOR



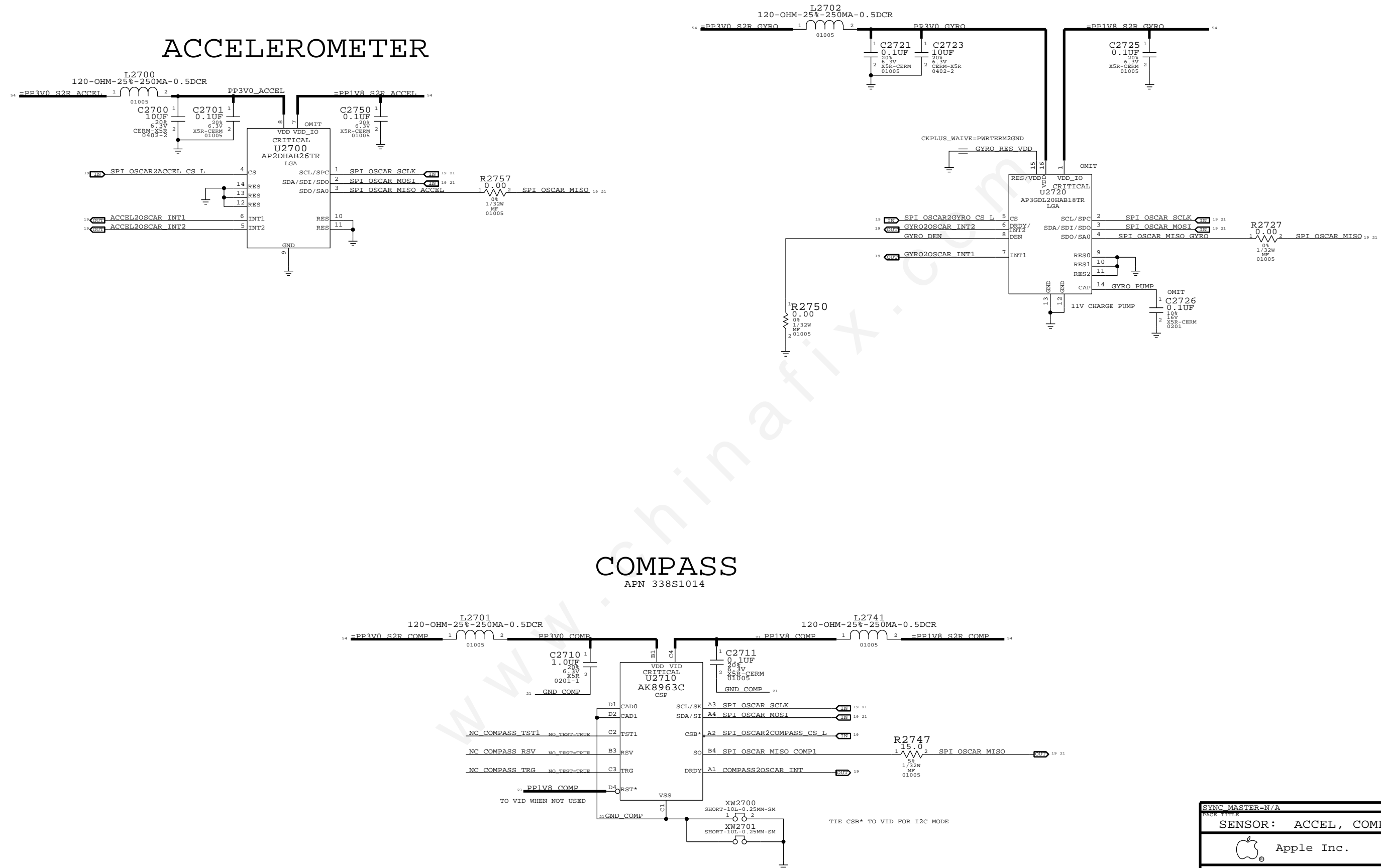
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# GYRO

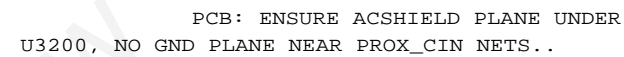
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
# COMPASS

APN 338S1014



PAGE TITLE		PAGE NUMBER	
SENSOR: ACCEL, COMPASS, GYRO		051-0886	
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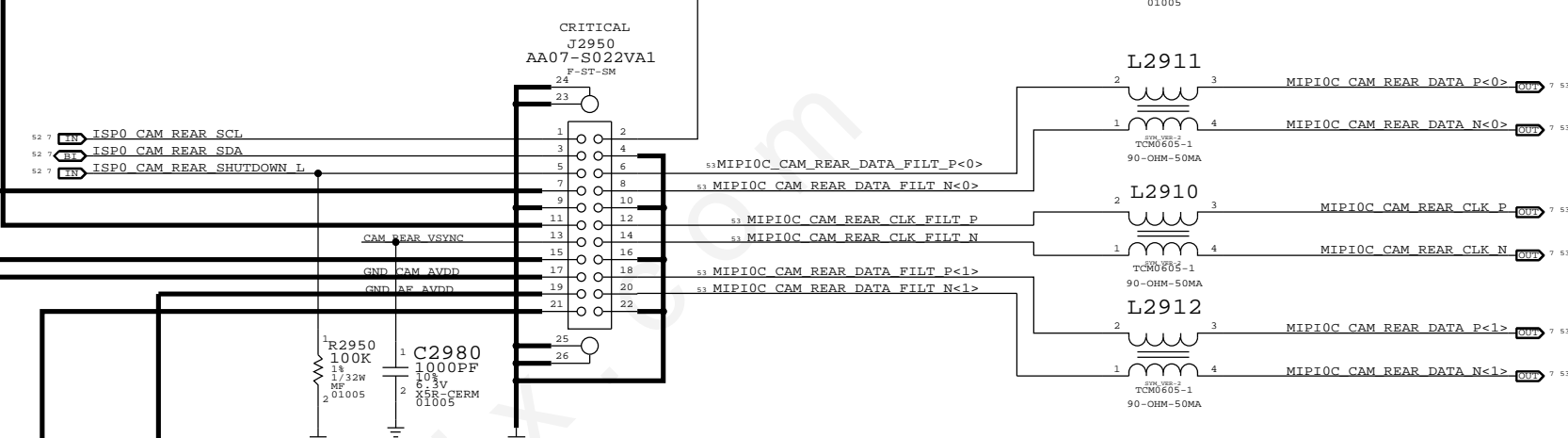
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# REAR CAMERA CONNECTOR

APN: 516S0973

PLUG: 516S0974



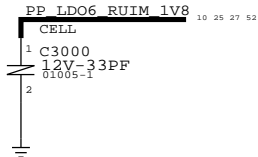
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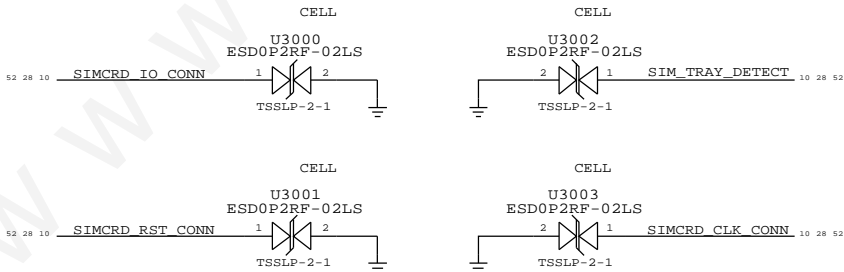
# AP INTERFACE & DEBUG CONNECTORS

## PROBE POINTS

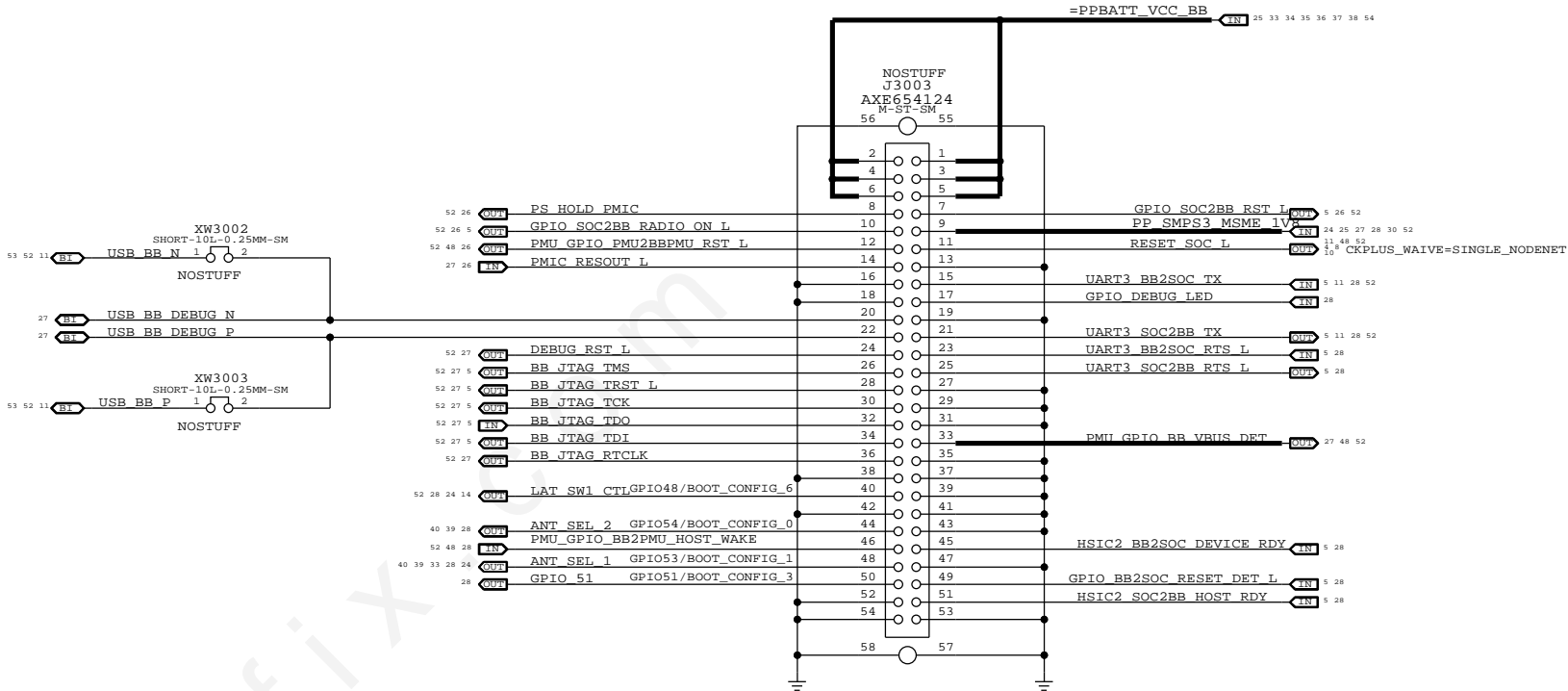
PP3000	P4MM	1	BB_ERROR_FLAG	28
PP3001	P4MM	1	SLEEP_CLK_32K	26 27
PP3002	P4MM	1	PMIC_SSBI	26 27
PP3003	P4MM	1	19P2M_MDM	26 27
PP3008	P4MM	1	WTR_SSBI_TX_GPS	28 29
PP3009	P4MM	1	WTR_SSBI_PRX_DRX	28 29
PP3010	P4MM	1	WTR_RX_ON	28 29
PP3011	P4MM	1	WTR_RF_ON	28 29
PP3012	P4MM	1	UART_WLAN2BB_LTE_COEX	28 44
PP3013	P4MM	1	UART_BB2WLAN_LTE_COEX	28 44



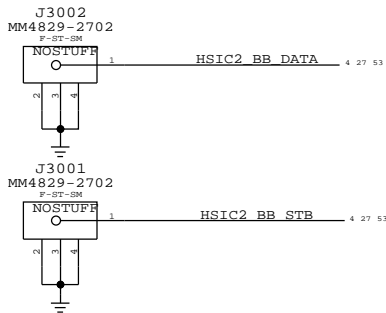
## SIM CARD ESD PROTECTION



## DEBUG CONNECTOR



BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION							
		6	5	4	3	2	1	0	
BOOT_DEFAULT_OPTION	0x00	X	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0x01	X	1	0	0	0	0	0	1
BOOT_HSIC_OPTION	0x02	X	1	0	0	0	0	1	0
BOOT_USB_OPTION	0x03	X	1	0	0	0	0	1	1
ENABLE_SAHARA_PROTOCOL	0x08	X	1	0	0	1	0	X	X



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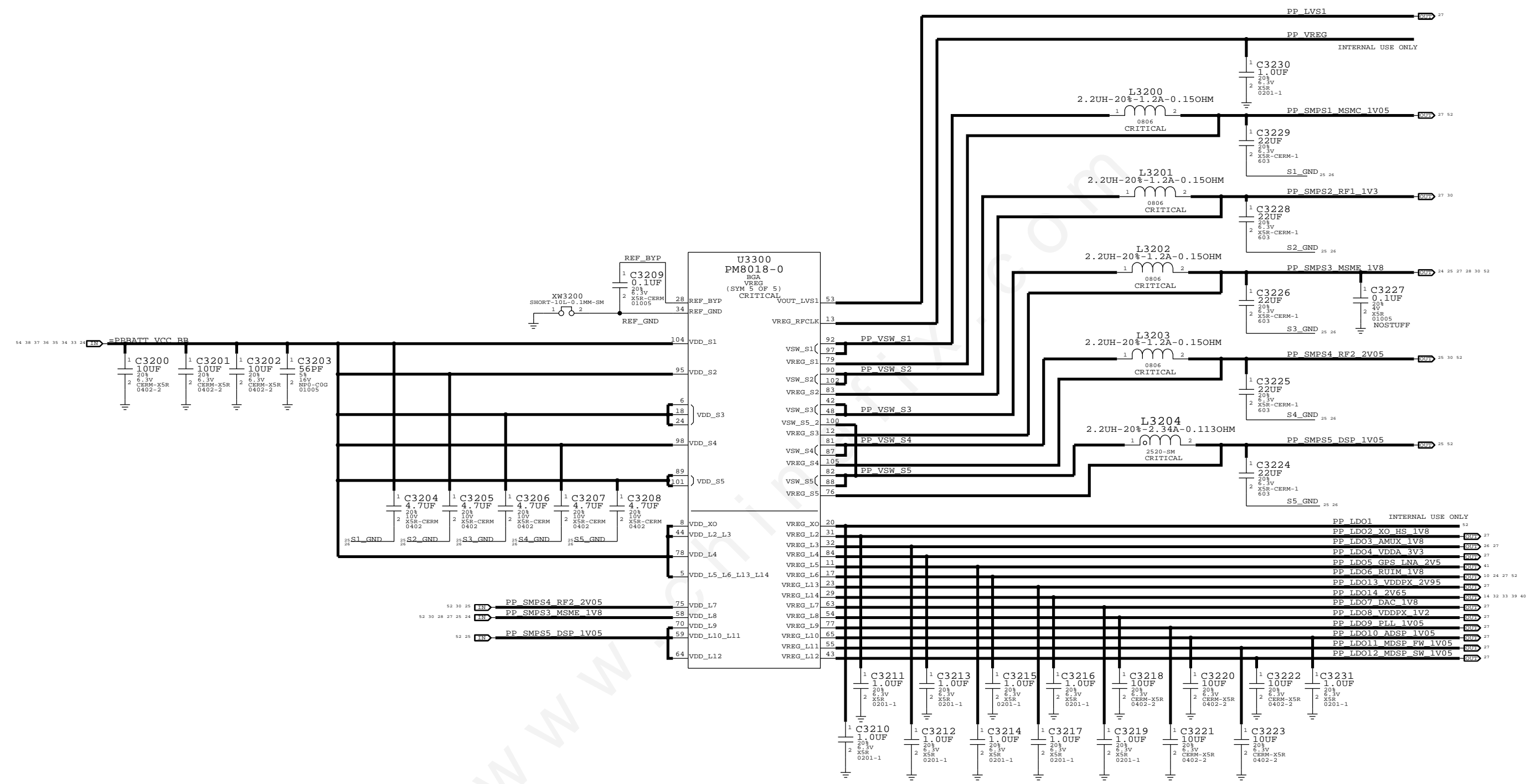
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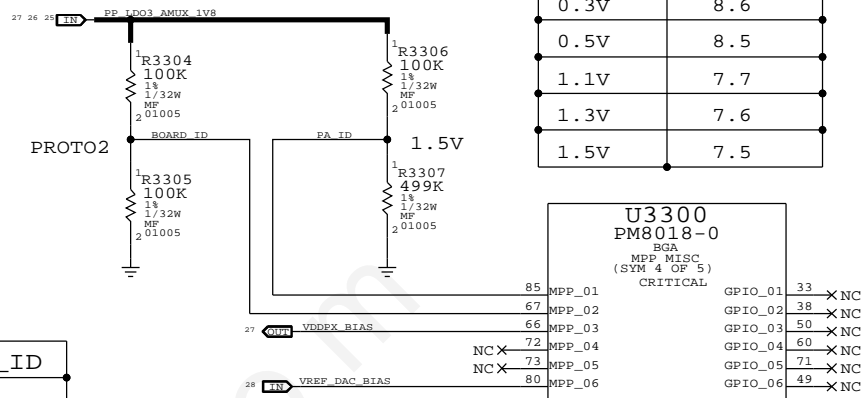
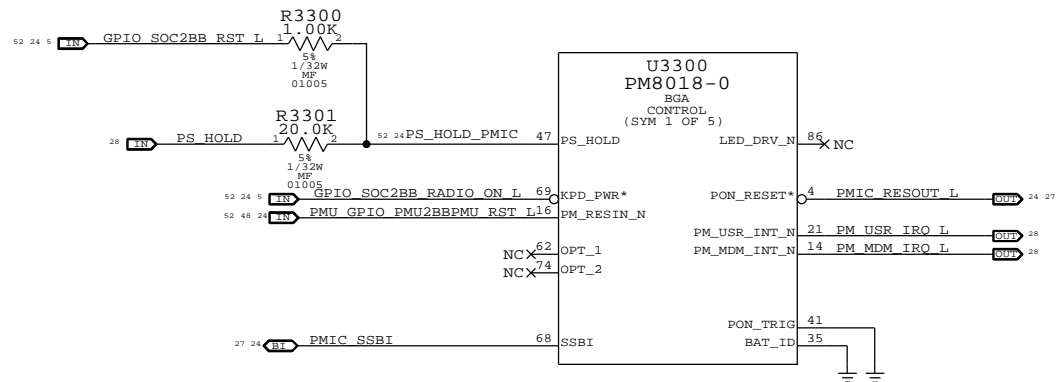


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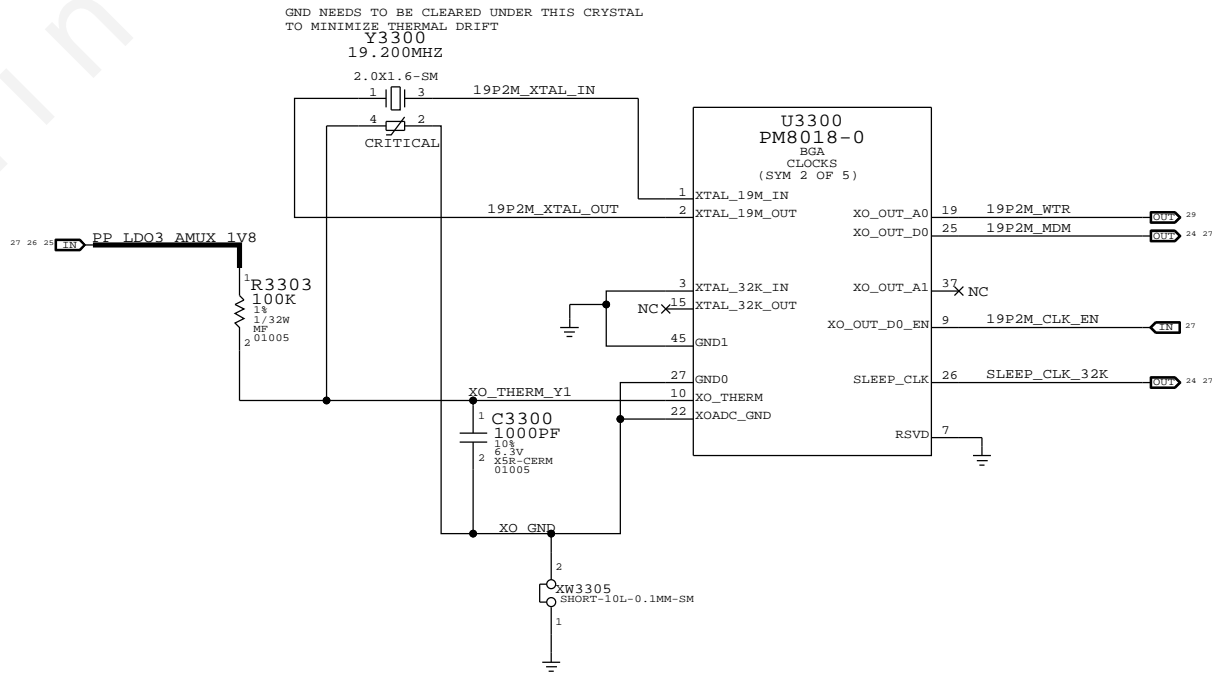
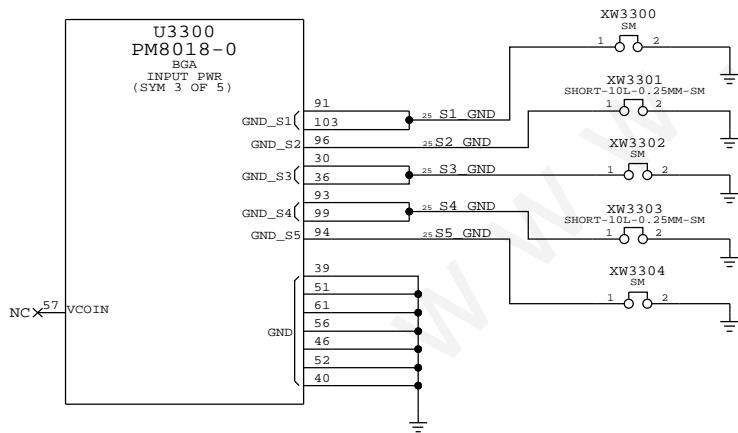
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0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5



AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



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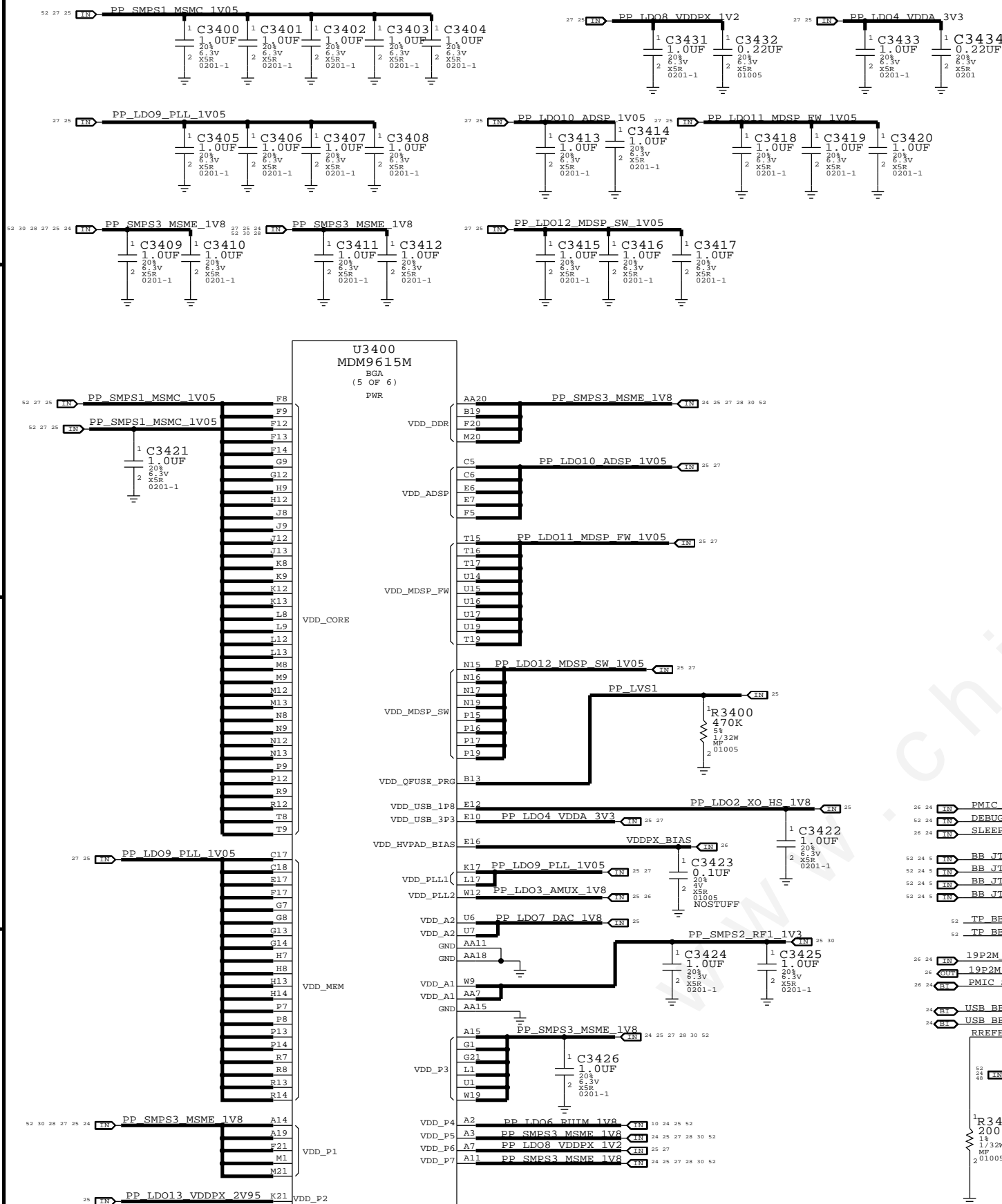
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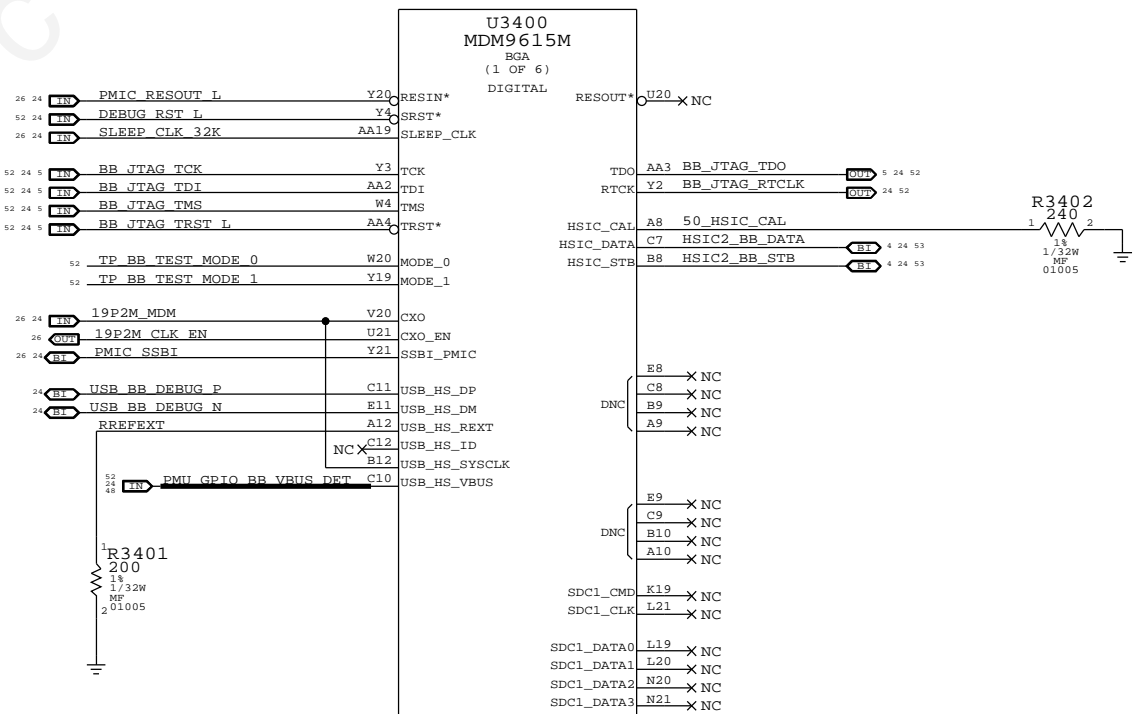
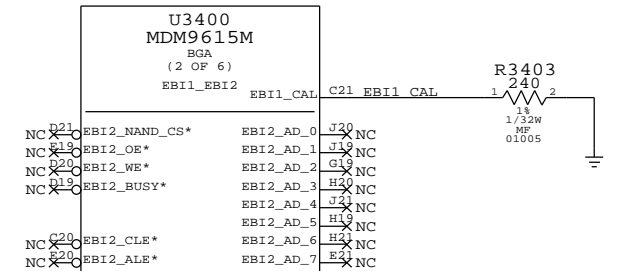
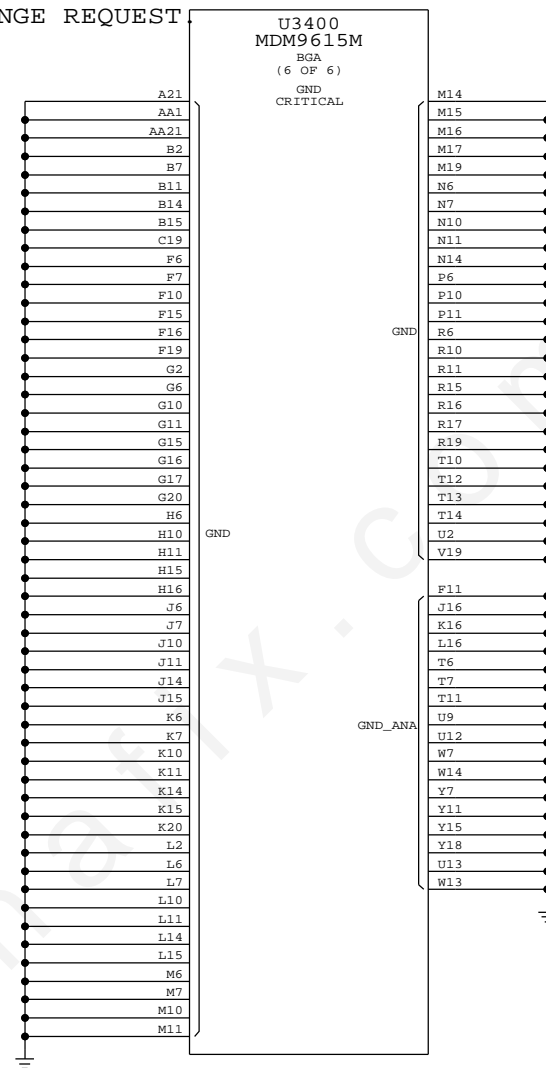
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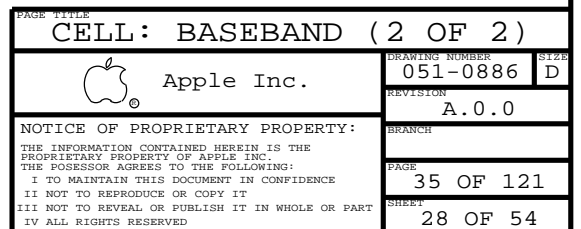
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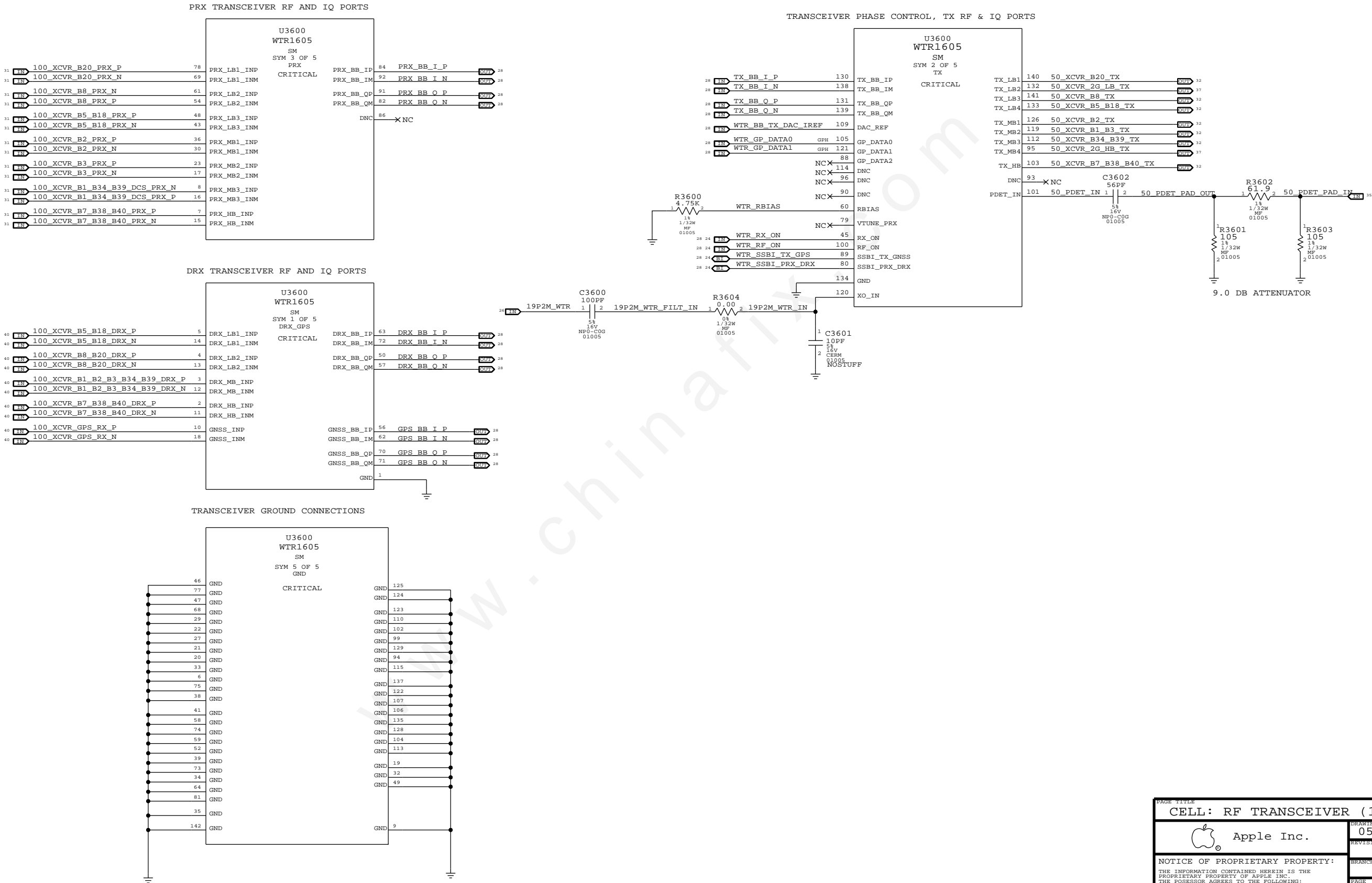
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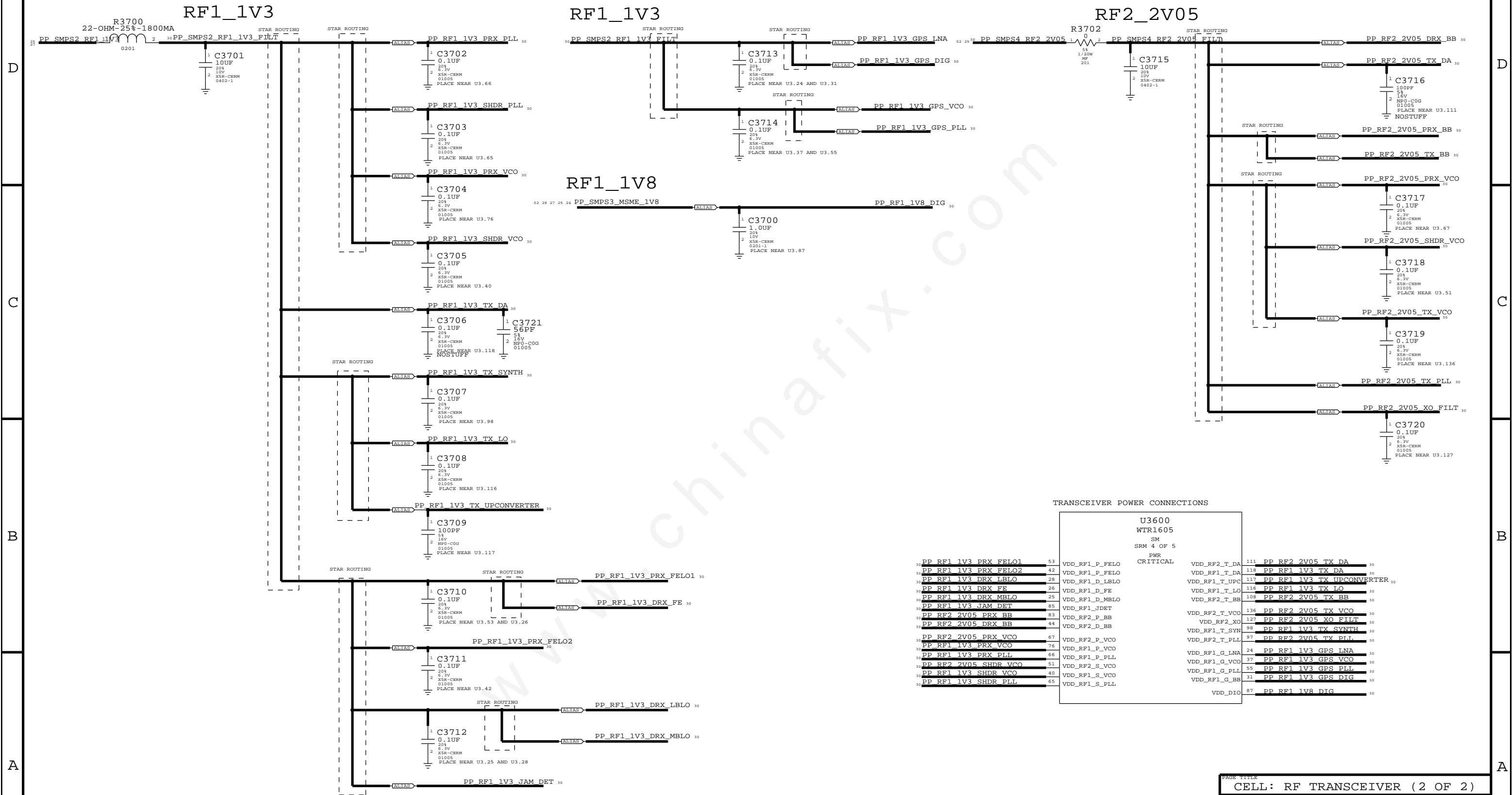
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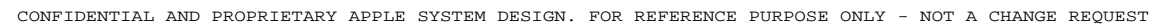


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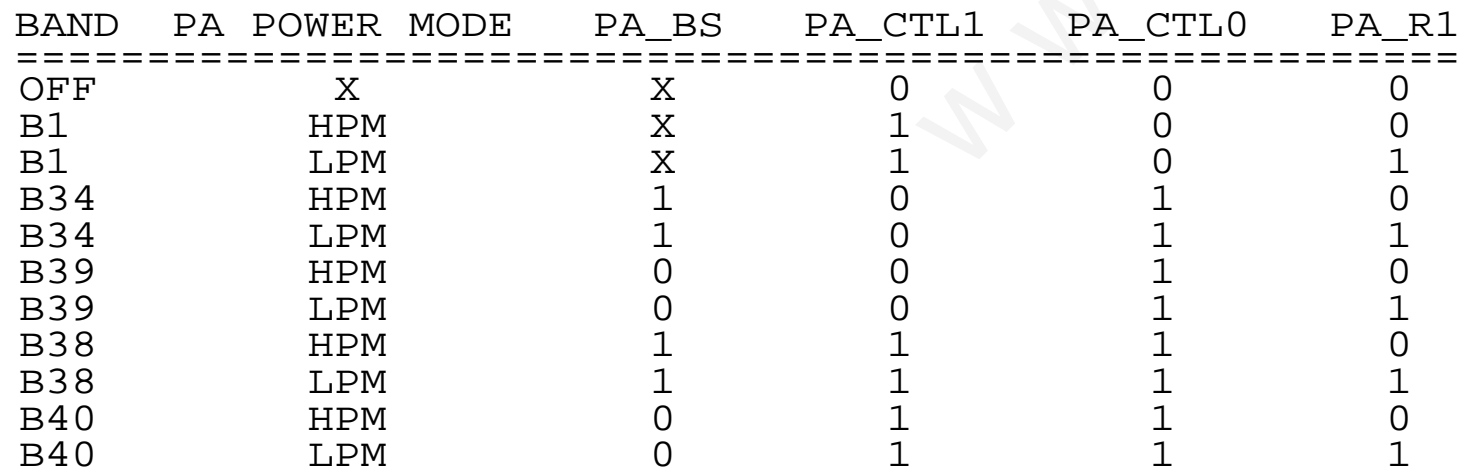



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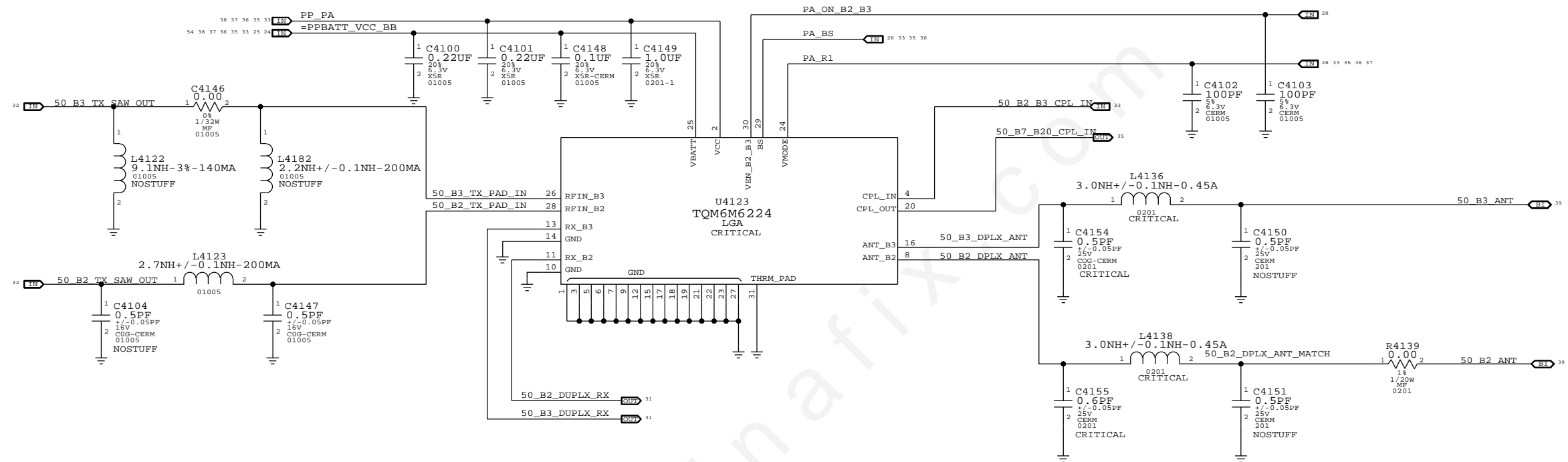
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# BAND 2 / 3 PAD

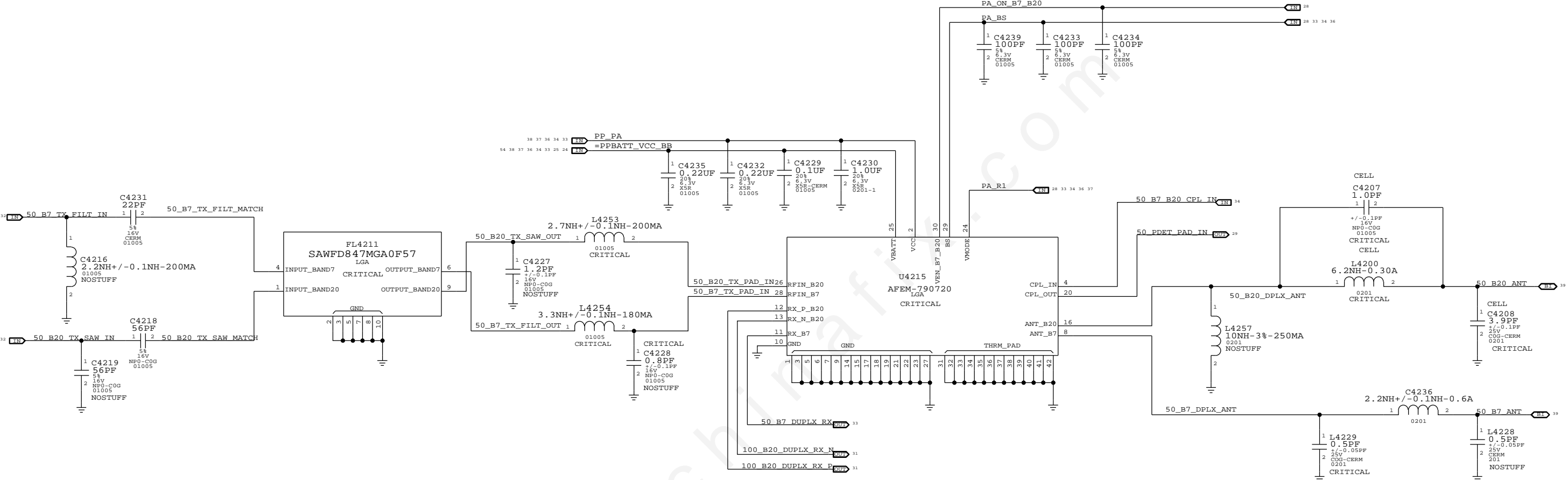


BAND	PA	POWER	MODE	PA_BS	PA_ON_B2_B3	PA_R1
=====	=====	=====	=====	=====	=====	=====
OFF		X		X	0	X
B3		HPM		0	1	0
B3		LPM		0	1	1
B2		HPM		1	1	0
B2		LPM		1	1	1


PAGE TITLE CELL: BAND 2/3 PAD		
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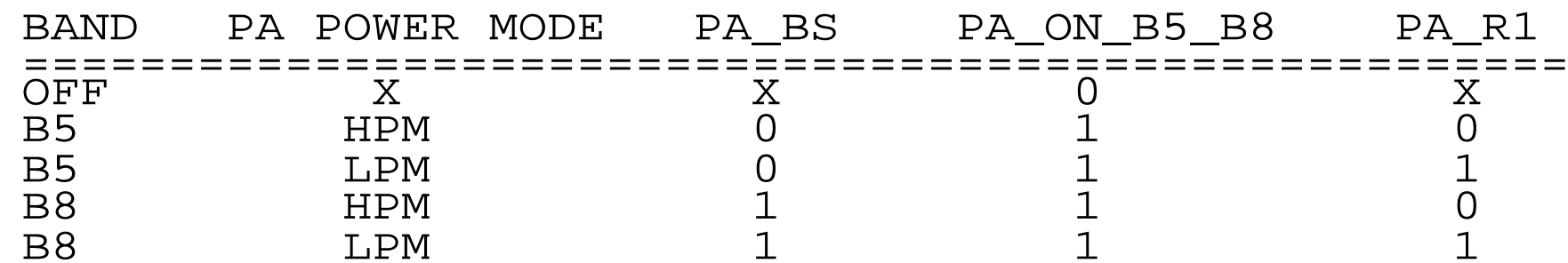



BAND 20/7 PAD



BAND	PA	POWER	MODE	PA_BS	PA_ON_B20_B7	PA_R1
=====	=====	=====	=====	=====	=====	=====
OFF	X			X	0	X
B20	HPM			0	1	0
B20	LPM			0	1	1
B7	HPM			1	1	0
B7	LPM			1	1	1

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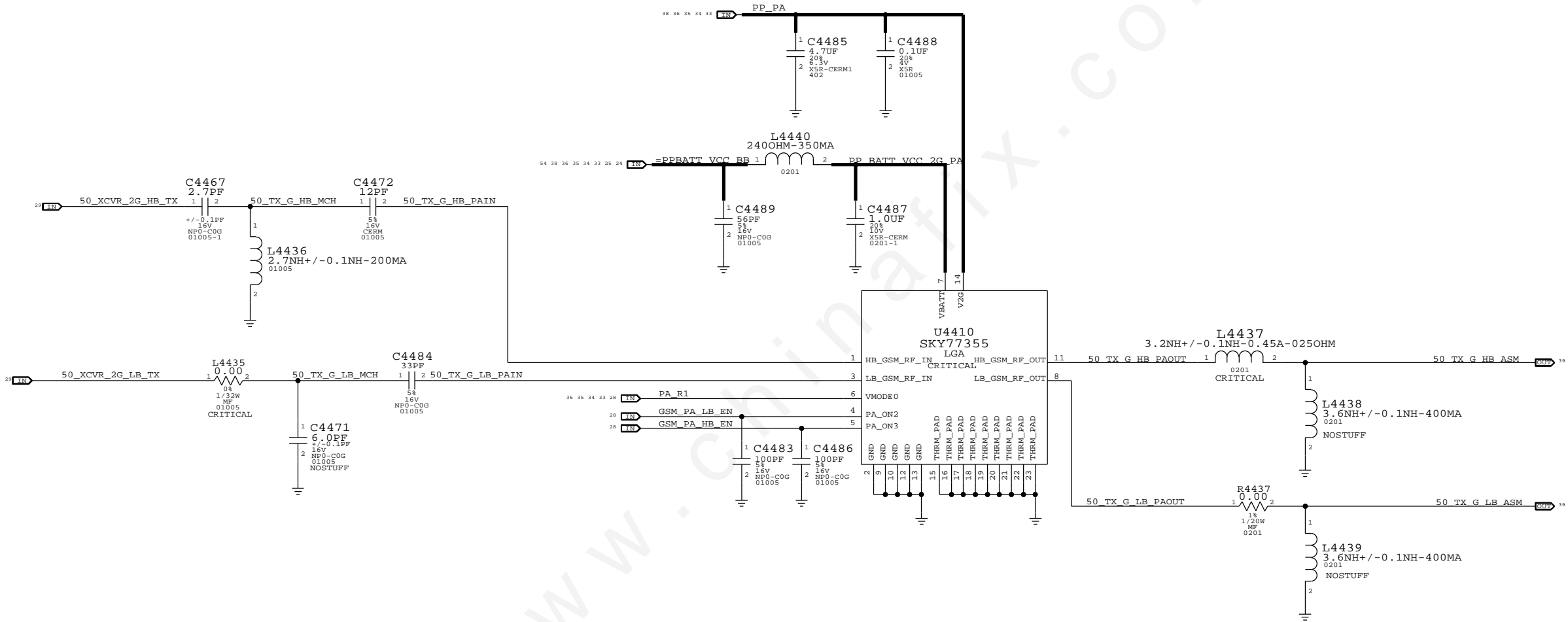



# 2G PA

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## 2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA_R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8

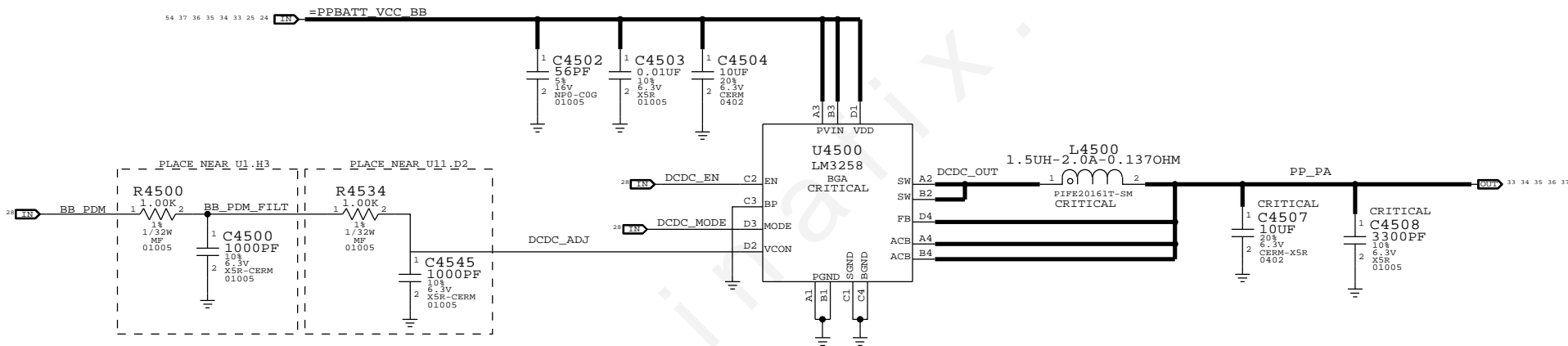



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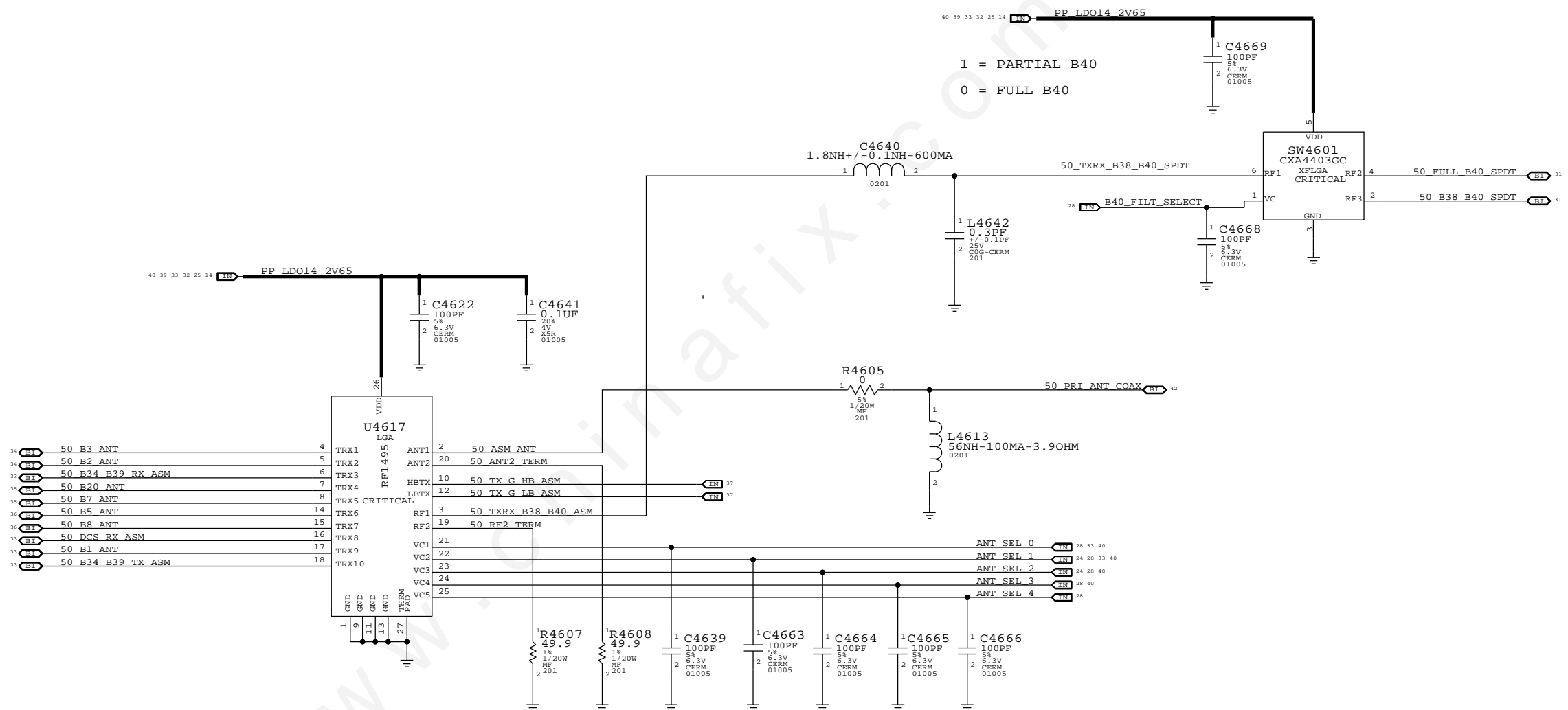



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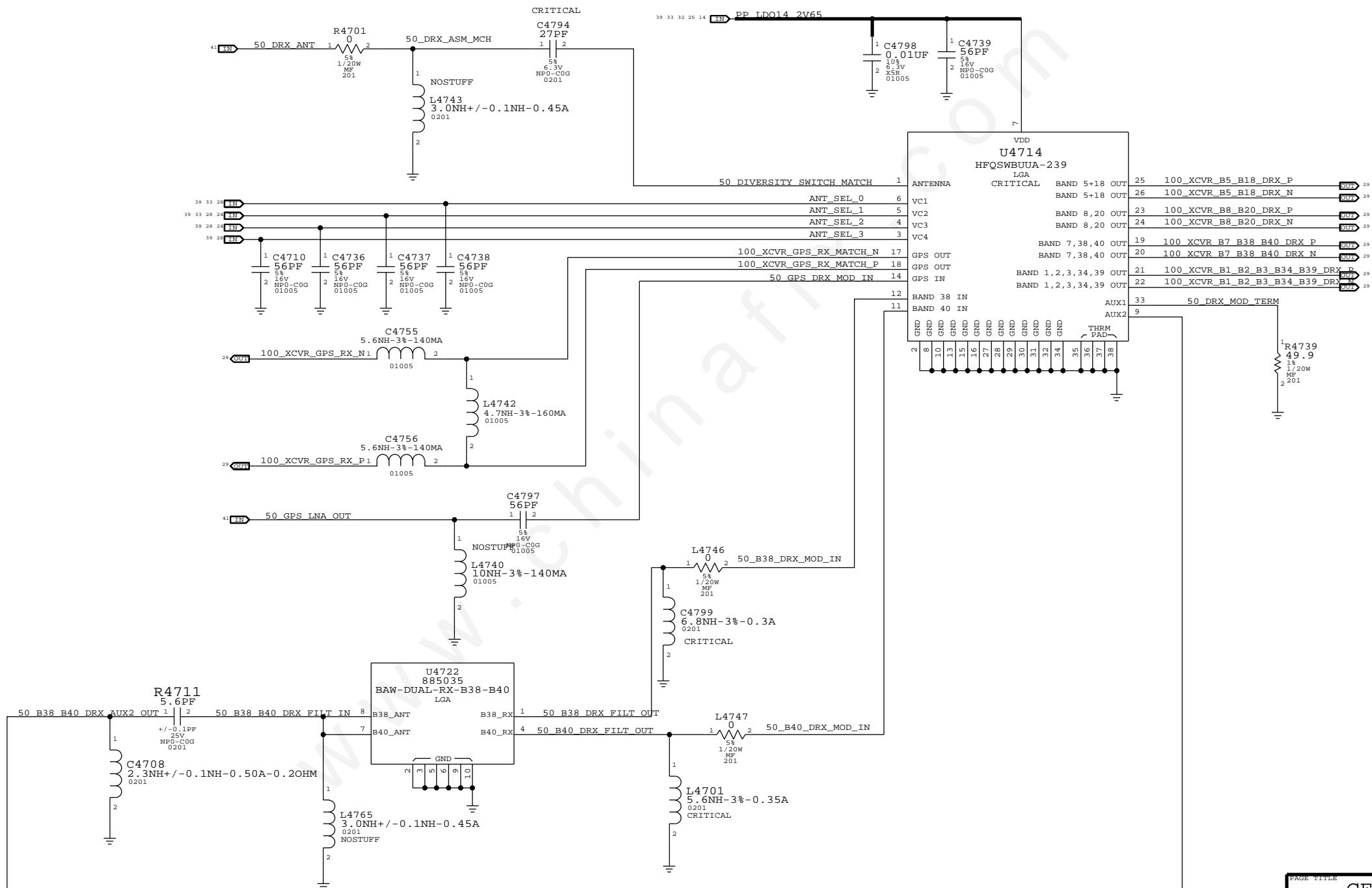
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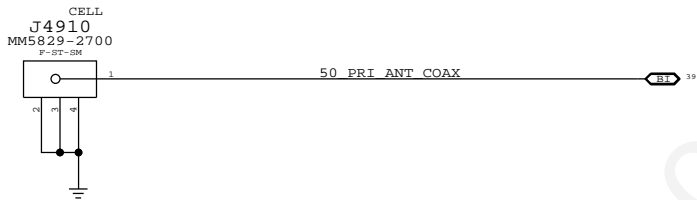



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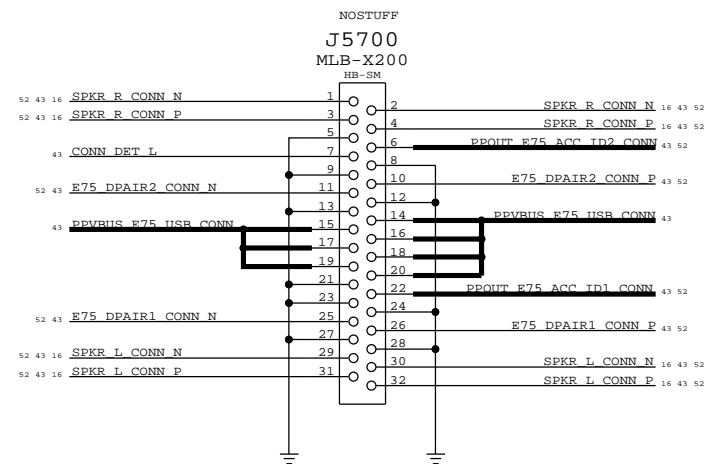


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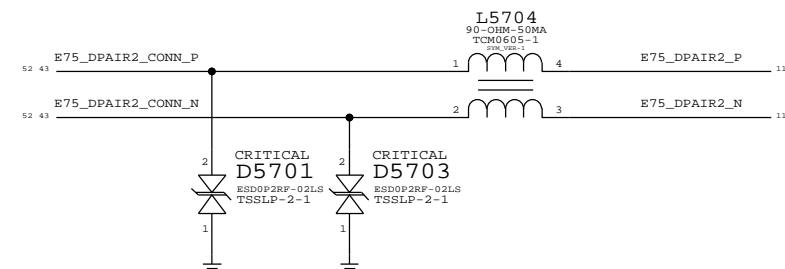
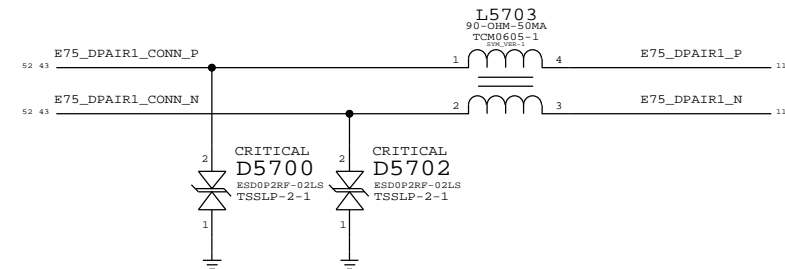
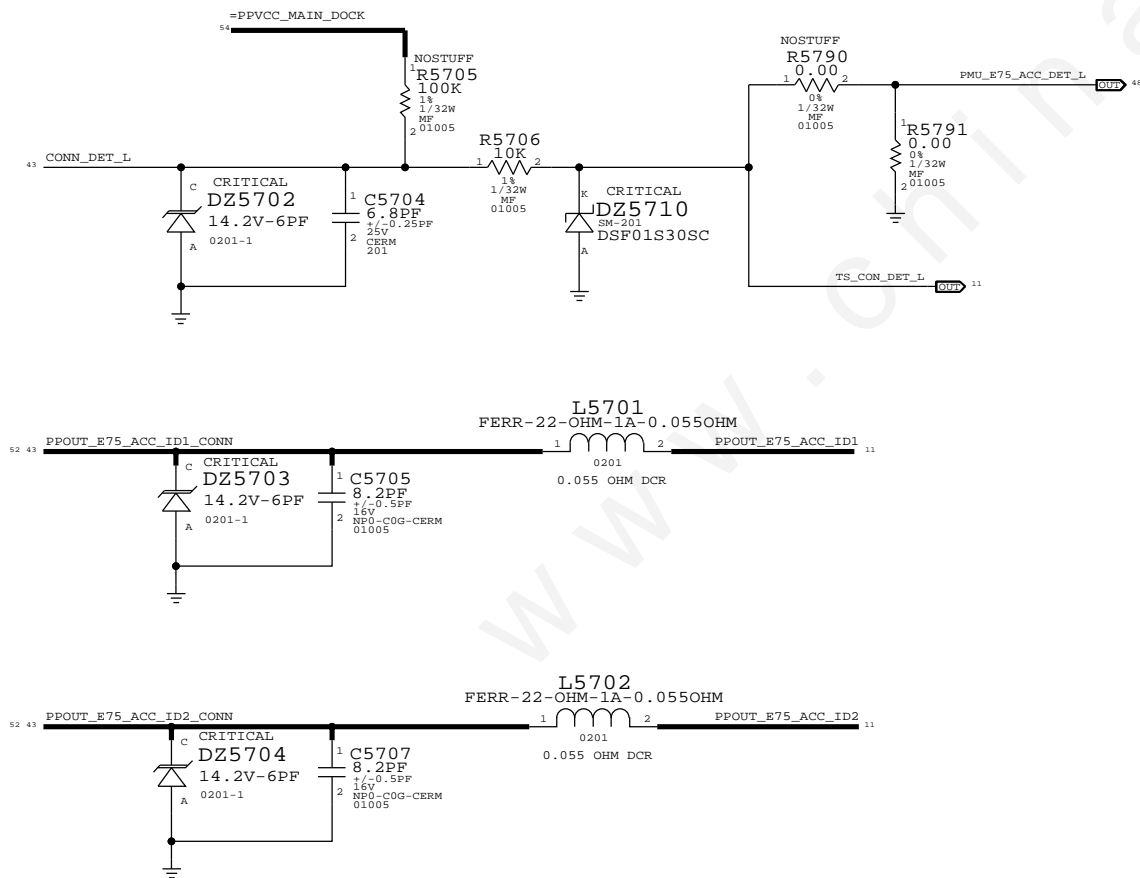
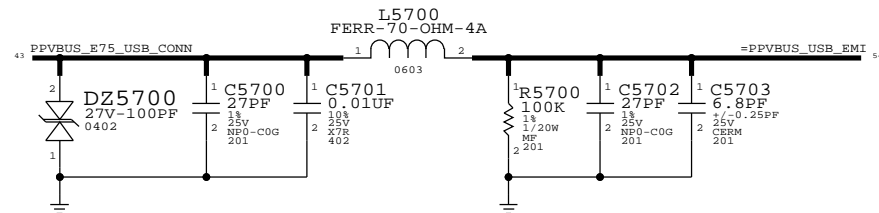
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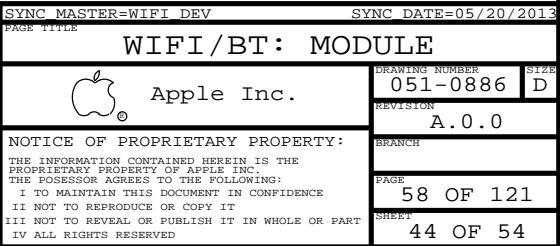
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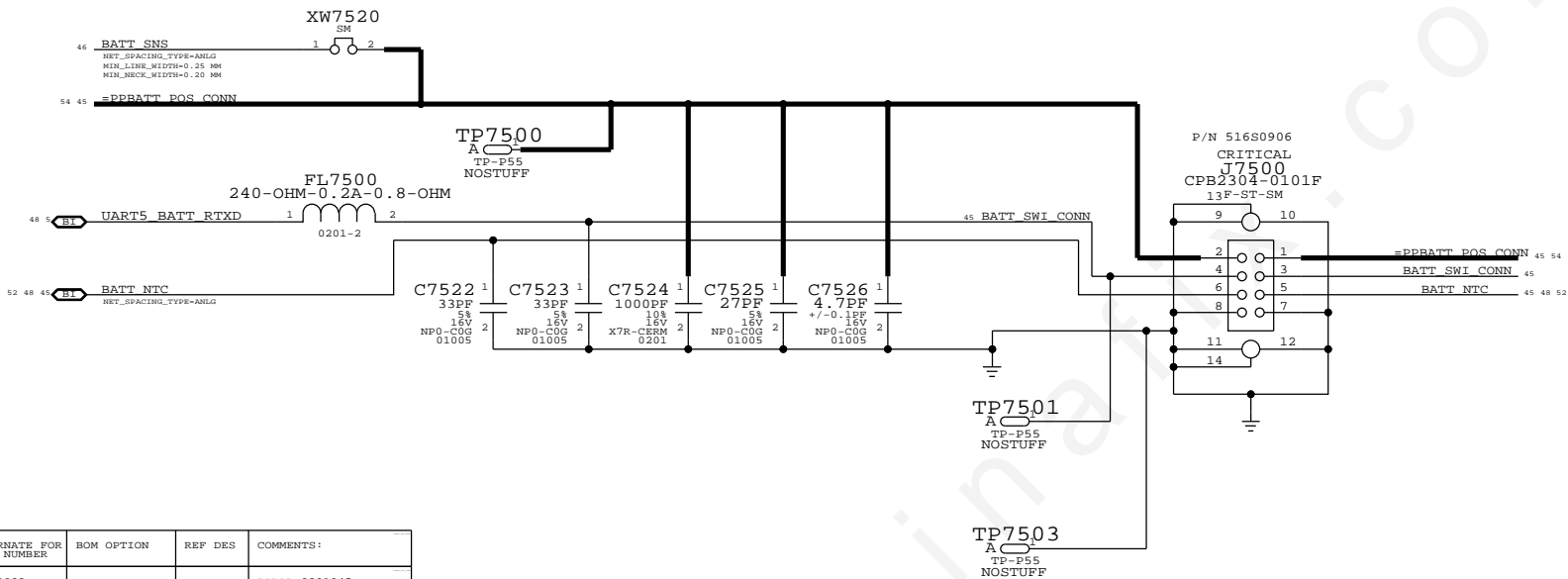


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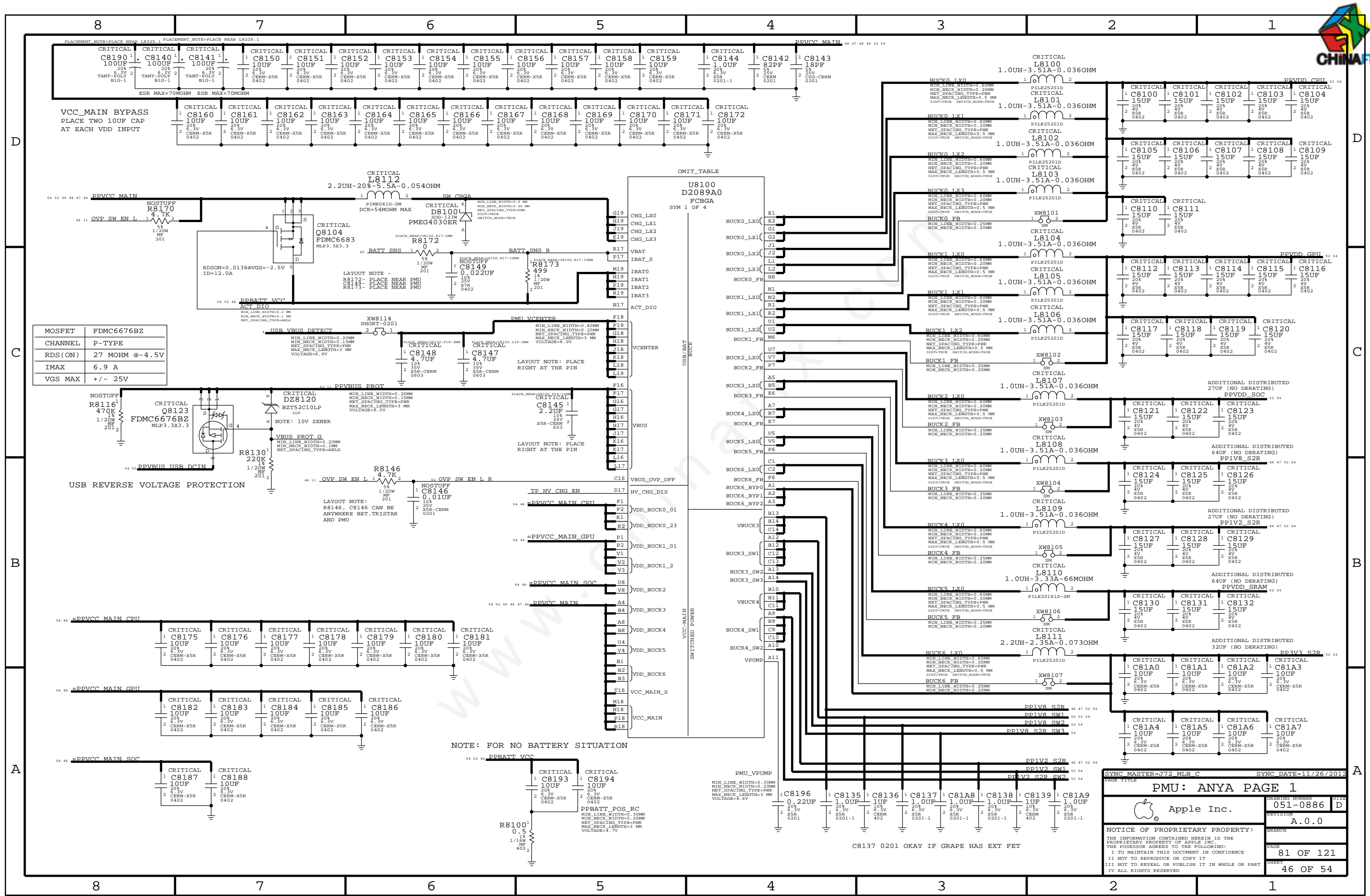
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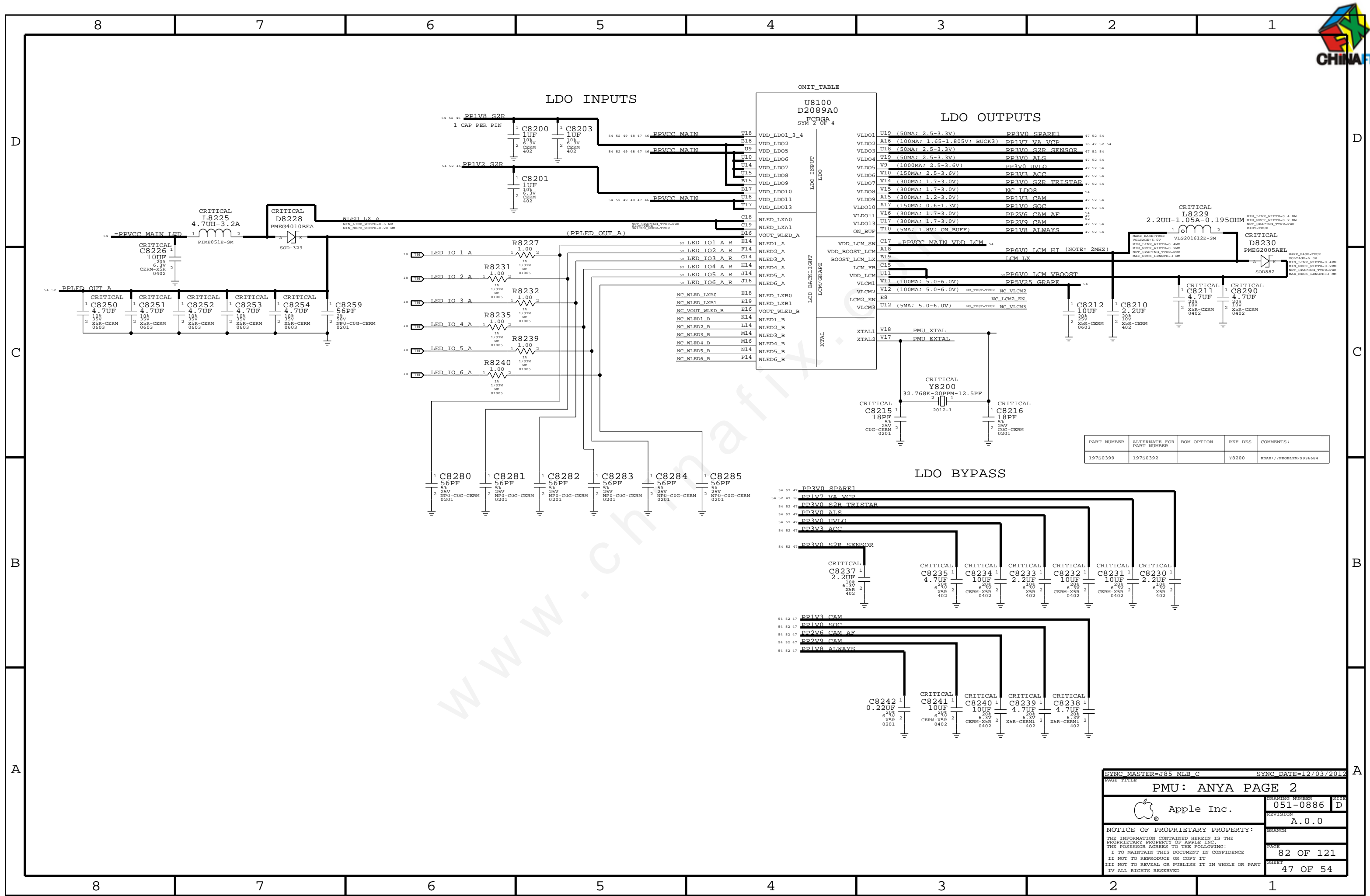
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MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

SYNC MASTER=J72 MLB C  
PAGE TITLE  
PMU: ANYA PAGE 1  
Apple Inc.  
DRAWING NUMBER 051-0886  
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR:///PROBLEM/9936684

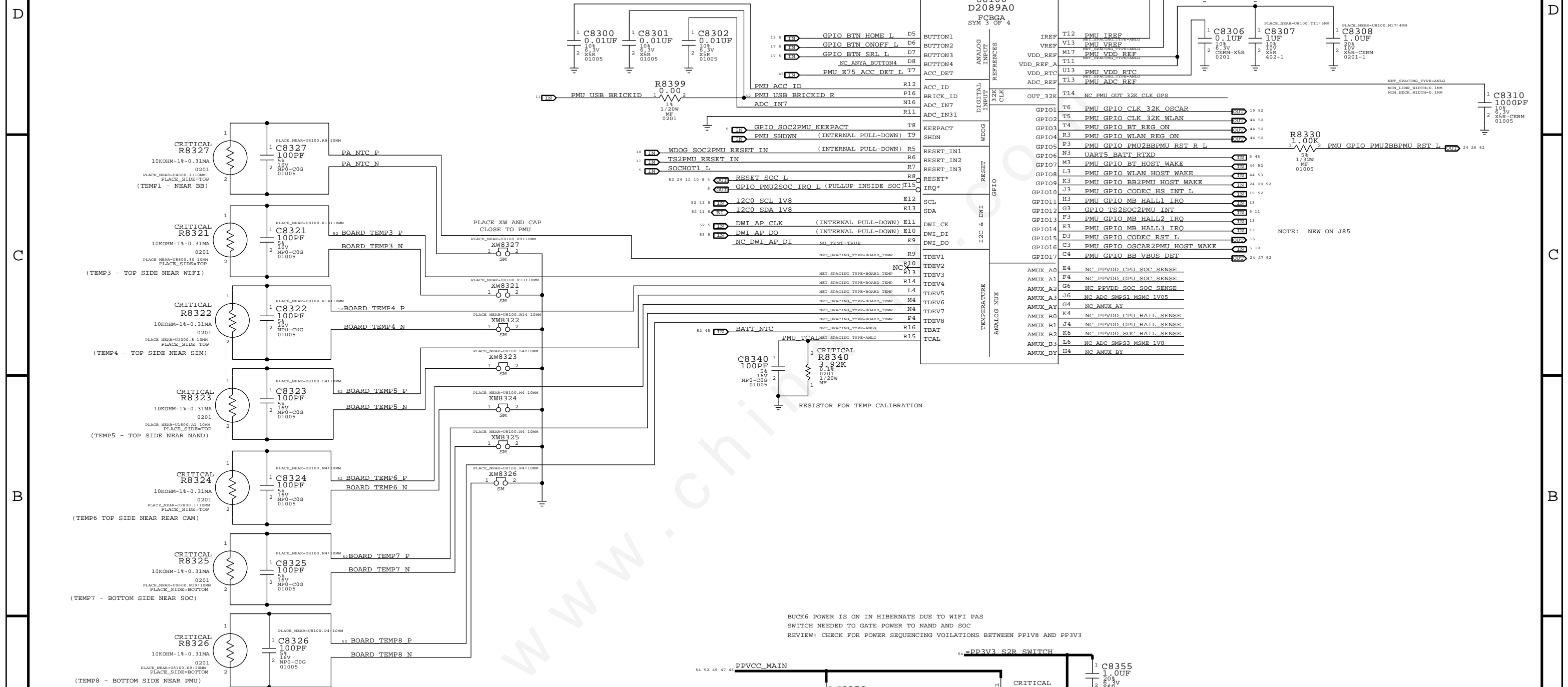
SYNC MASTER=J85 MLB C		SYNC DATE=12/03/2012	
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PMU: ANYA PAGE 2			
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		SIZE	D
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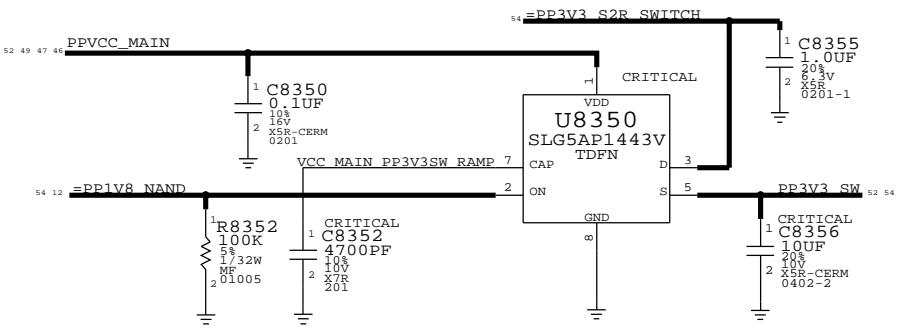
REVIEW: VERIFY NC ON TDEV2 IS OK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706		C8308	

I2C ADDRESS: 0111100X (0X78)

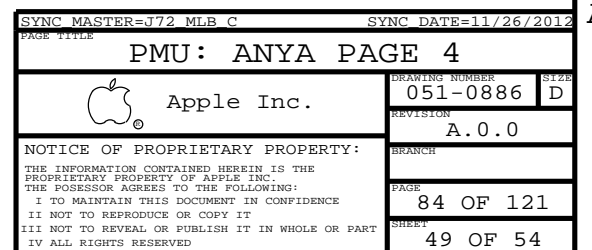


BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS  
SWITCH NEEDED TO GATE POWER TO NAND AND SOC  
REVIEW: CHECK FOR POWER SEQUENCING VIOLATIONS BETWEEN PP1V8 AND PP3V3



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	R8321, R8322	R8323, R8324	RDAR: // PROBLEM/8380167
118S0764	118S0717		R8340	RDAR: // PROBLEM/8380167

PAGE TITLE		SYNC DATE=11/26/2012	
PMU: ANYA PAGE 3		DRAWING NUMBER	051-0886
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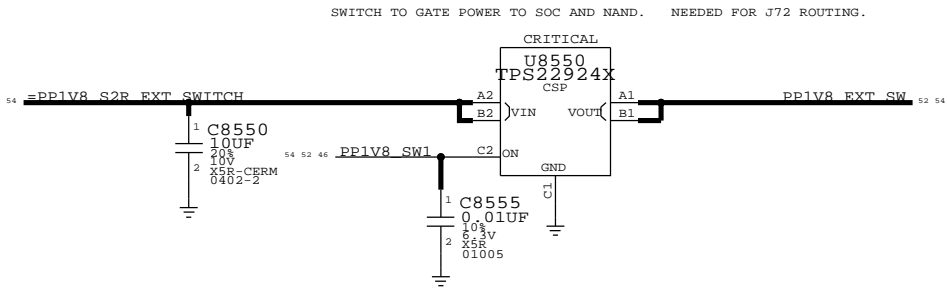
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SYNC MASTER=J85 MLB C		SYNC DATE=11/26/2012	
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POWER: PP1V8_SW			
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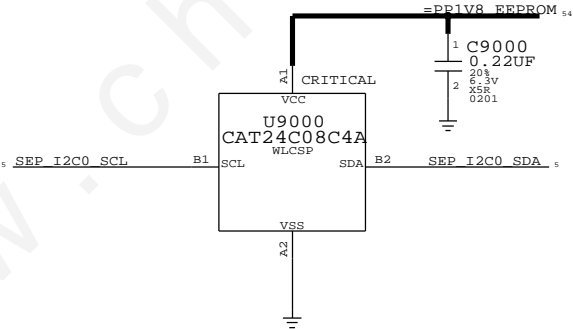



DEBUG

TP9002  
TP-P55

SEP EEPROM


UNPROGRAMMED P/N: 335S0894



SYNC MASTER=J72 MLB C		SYNC DATE=11/26/2012	
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SEP: EEPROM & SOC DEBUG			
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8	7	6	5	4	3	2	1
TP9300 GPIO CODEC IRO L 5 15 TP9304 PMU GPIO CODEC HS INT L 15 48 TP9303 BATT NTC 45 48 TP9305 PPLED OUT A 47 54 TP9396 PP3V0 UVLO 47 54 TP9397 PP3V0 SPARE1 47 54 TP9398 SOCHOT0 L 5 49 TP9312 BOARD TEMP3 P 48 TP9313 BOARD TEMP4 P 48 TP9314 BOARD TEMP5 P 48 TP9315 BOARD TEMP6 P 48 TP9316 BOARD TEMP7 P 48 TP9317 BOARD TEMP8 P 48 TP9318 CLK 32K SOC2CUMULUS 5 13 TP9320 CODEC HP DET R 15 TP9321 CODEC HP HS3 15 TP9322 CODEC HP HS3 REF 15 TP9323 CODEC HP HS4 15 TP9324 CODEC HP HS4 REF 15 TP9325 CODEC HP LEFT 15 TP9326 CODEC HP RIGHT 15 TP9328 DISPLAY SYNC R 13 TP9329 DWI AP CLK 5 48 TP9330 E75 DPAIR1 CONN N 43 TP9331 E75 DPAIR1 CONN P 43 TP9332 E75 DPAIR2 CONN N 43 TP9333 E75 DPAIR2 CONN P 43 TP9334 FMIO CE0 L 6 12 TP9335 FMIO CE0 L 6 12 TP9336 GND TP9337 GND AUDIO CODEC 15 TP9338 GPIO BTN HOME FILT L 13 TP9339 GPIO BTN ONOFF L FILT 17 TP9340 GPIO BTN SRL L FILT 17 TP9341 GPIO BTN VOL DOWN L FILT 17 TP9342 GPIO BTN VOL UP L FILT 17 TP9343 GPIO FORCE DFU 5 TP9344 GPIO GRAPE IRO L 5 13 TP9345 GPIO GRAPE RST L 5 13 TP9346 GPIO SOC2BB WAKE MODEM 5 28 TP9347 GPIO SPKAMP KEEPALIVE 5 16 TP9348 I2C0_SCL_1V8 5 11 48 TP9349 I2C0_SDA_1V8 5 11 48 TP9350 I2C2_SCL_1V8 5 16 TP9351 I2C2_SDA_1V8 5 16 TP9352 ISP0 CAM REAR CLK 7 23 TP9353 ISP0 CAM REAR_SCL 7 23 TP9354 ISP0 CAM REAR_SDA 7 23 TP9355 ISP0 CAM REAR_SHUTDOWN L 7 23 TP9356 ISP1 CAM FRONT CLK 7 20 TP9357 ISP1 CAM FRONT_SCL 7 20 TP9358 ISP1 CAM FRONT_SDA 7 20 TP9359 ISP1 CAM FRONT_SHUTDOWN L 7 20 TP9360 JTAG SOC SEL 4 10 TP9361 JTAG SOC TCK 4 11 TP9362 JTAG SOC TDI 4 TP9363 JTAG SOC TMS 4 11 TP9364 JTAG SOC TRST L 4 10 TP9365 JTAG WLAN SEL 44 TP9366 OSCAR2RADIO CONTEXT A 19 28 44 TP9367 OSCAR2RADIO CONTEXT B 19 28 44 TP9368 WLAN TX BLANK 28 44 TP9369 LAT SW1 CTL 14 24 28 TP9370 LAT SW2 CTL 14 28 TP9371 LED IO1 A R 47 TP9372 LED IO2 A R 47 TP9373 LED IO3 A R 47 TP9374 LED IO4 A R 47 TP9375 LED IO5 A R 47 TP9376 LED IO6 A R 47 TP9377 MIKEY TS N 11 15 TP9378 MIKEY TS P 11 15	TP9380 OVP SW EN L R 46 TP9382 PMU GPIO BT HOST WAKE 44 48 TP9383 PMU GPIO BT REG ON 44 48 TP9384 PMU GPIO CLK 32K OSCAR 19 48 TP9385 PMU GPIO CLK 32K WLAN 44 48 TP9387 PMU USB BRICKID R 48 TP9388 PP1V0 SOC 47 54 TP9389 PP1V2 S2R 46 47 54 TP9390 PP1V2 S2R SW2 46 54 TP9391 PP1V2 SW1 46 54 TP9393 PP1V7 VA VCP 16 47 54 TP9395 PP1V8 ALWAYS 47 54 TP93A0 PP1V8 EXT SW 50 54 TP93A1 PP1V8 GRAPE FILT 13 TP93A2 PP1V8 GRAPE SW 13 TP93A3 PP1V8 PLL SOC F 4 TP93A4 PP1V8 S2R 46 47 54 TP93A6 PP1V8 S2R SW3 COMP 54 TP93A7 PP1V8 SW1 46 50 54 TP93A8 PP1V8 SW2 46 54 TP93A9 PP1V8 XTAL 8 TP93B0 PP2V6 CAM AF 47 54 TP93B8 PP3V0 S2R HALL FILT 13 TP93C0 PP3V0 S2R SENSOR 47 54 TP93C1 PP3V0 S2R TRISTAR 47 54 TP93C3 PP3V3 ACC 47 54 TP93C4 PP3V3 S2R 46 54 TP93C5 PP3V3 SW 48 54 TP93C6 PP5V25 GRAPE FILT 13 TP93C8 PP6V0 LCM VBOOST 47 TP93C9 PPBATT VCC 46 54 TP93D0 PPLED BACK REG A 18 TP93D1 PPOUT E75 ACC ID1 CONN 43 TP93D2 PPOUT E75 ACC ID2 CONN 43 TP93D3 PPVBUS PROT 11 46 TP93D4 PPVBUS USB DCIN 46 54 TP93D5 PPVCC MAIN 46 47 48 49 54 TP93D6 PPVCC MAIN LCD SW CONN 18 TP93D7 PPVDD CPU 46 54 TP93D8 PPVDD GPU 46 54 TP93D9 PPVDD SOC 46 54 TP93E0 PPVDD SRAM 46 54	TP93G4 PP SMPS4 RF2 2V05 25 30 TP93G9 SOC TESTMODE 4 10 TP93H1 SPI1 GRAPE CS L 5 13 TP93H2 SPI1 GRAPE MISO 5 13 TP93H3 SPI1 GRAPE MOSI 5 13 TP93H4 SPI1 GRAPE SCLK R 13 TP93H5 SPKR L CONN N 16 43 TP93H6 SPKR L CONN P 16 43 TP93H7 SPKR R CONN N 16 43 TP93H8 SPKR R CONN P 16 43 TP93I1 TP JTAG SOC TDO 4 TP93I2 TP JTAG WLAN TCK 44 TP93I3 TP JTAG WLAN TRST L 44 TP93I4 UART0 SOC RXD 5 11 TP93I5 UART0 SOC TXD 5 11 TP93I6 UART3 BB2SOC TX 5 11 24 28 TP93I7 UART3 SOC2BB TX 5 11 24 28 TP93I8 UART6 TS ACC RXD 5 11 TP93I9 UART6 TS ACC TXD 5 11 TP93J0 USB SOC N 4 11 TP93J1 USB SOC P 4 11 TP93J9 PP3V0 ALS 47 54 TP93JA PP2V9 CAM 47 54 TP93JB PP1V3 CAM 47 54 TP93JC PMU GPIO WLAN REG ON 44 48	RF TEST POINTS TP93G1 PP SMPS1 MSMC 1V05 25 27 TP93G2 PP SMPS3 MSME 1V8 24 25 27 28 30 TP93G5 PP SMPS5 DSP 1V05 25 TP93H1 PP LDO1 25 TP93H5 TP BB TEST MODE 0 27 TP93I0 TP BB TEST MODE 1 27 TP93J0 SIMCRD RST CONN 10 24 28 TP93J5 SIMCRD CLK CONN 10 24 28 TP93J7 SIMCRD IO CONN 10 24 28 TP93J8 SIM TRAY DETECT 10 24 28 TP93J9 PP LDO6 RUIM 1V8 10 24 25 27 TP93J2 GPIO SOC2BB RADIO ON L 5 24 26 TP93J3 GPIO SOC2BB RST L 5 24 26 TP93J4 PMU GPIO PMU2BBPMU RST L 24 26 48 TP93J5 PMU GPIO BB2PMU HOST WAKE 24 28 48 TP93J6 PS HOLD PMIC 24 26 TP93J7 DEBUG RST L 24 27 TP93J8 BB JTAG RTCLK 24 27 TP93J9 BB JTAG TCK 5 24 27 TP93J0 BB JTAG TDI 5 24 27 TP93J1 BB JTAG TDO 5 24 27 TP93J2 BB JTAG TMS 5 24 27 TP93J3 BB JTAG TRST L 5 24 27 TP93J4 USB BB N 11 24 53 TP93J5 USB BB P 11 24 53 TP93J6 RESET SOC L 4 8 10 11 24 48 TP93J7 PMU GPIO BB VBUS DET 24 27 48	STANDOFFS: P/N 860-1657 STD9300 STDOFF-3.3X1.8R1.28H-SM STD9301 STDOFF-3.3X1.8R1.28H-SM STANDOFF: P/N 860-1683 STD9302 STDOFF-3.3X2.2R1.35H-SM-1 PLATED THROUGH HOLES DRILL SIZE: 1.1MM X 0.4MM PLATING SIZE: 1.4MM X 0.7MM SL9300 TH-NSP SL-1.1X0.4-1.4X0.7 SL9303 TH-NSP SL-1.1X0.4-1.4X0.7 SL9304 TH-NSP SL-1.1X0.4-1.4X0.7 SL9305 TH-NSP SL-1.1X0.4-1.4X0.7 MH9300 3P25R2P5 860-1688 MH9302 WASHER-BTN-MLB-X221 TH NEAR BUTTON FLEX CONN			

SYNC MASTER=J85 MLB C		SYNC DATE=12/03/12	
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87654321

EE CHARACTERIZATION TP

FOR FRANK (SEG)

NAND

PP9401	1	FMI0_DQS	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.D34:2MM	4 12 53
PP9402	1	FMI0_AD<3>	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.C34:2MM	6 12
PP9403	1	FMI0_DQS	PLACE_NEAR=U0652.D34:2MM	4 12 53
PP9410	1	TP_TCKC_U1400		12
PP9411	1	TP_TM5C_U1400		12
PP9412	1	TP_U1400_RB0		12
PP9413	1	TP_U1400_RB1		12

DWI

PP9405	1	DWI_AP_DO	PLACE_SIDE=BOTTOM PLACE_NEAR=U8100:2MM	5 48
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AUDIO

PP9406	1	I2S0_CODEC_ASP_MCK	PLACE_NEAR=U1900:2MM	5 15
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PP9416	1	I2S2_CODEC_XSP_LRCK	PLACE_NEAR=U1900:2MM	5 15
PP9417	1	I2S2_CODEC_XSP_DOUT	PLACE_NEAR=U1900:2MM	5 15

PP9419	1	I2S1_SPKAMP_MCK	PLACE_NEAR=U2040:2MM	5 16
PP9420	1	I2S1_SPKAMP_BCLK	PLACE_NEAR=U2040:2MM	5 16
PP9421	1	I2S1_SPKAMP_LRCK	PLACE_NEAR=U2040:2MM	5 16
PP9422	1	I2S1_SPKAMP_DOUT	PLACE_NEAR=U2040:2MM	5 16
PP9423	1	I2S1_SPKAMP_DIN	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	5 16

PP9424	1	SPI2_CODEC_SCLK	PLACE_NEAR=U1900:2MM	5 15
PP9425	1	SPI2_CODEC_MOSI	PLACE_NEAR=U1900:2MM	5 15
PP9426	1	SPI2_CODEC_MISO	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	5 15

GRAPE

OSCAR

PP9428	1	UART4_SOC2OSCAR_TXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U2400:2MM	5 19
PP9429	1	UART4_OSCAR2SOC_RXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	5 19

UART5

CAMERA

PP9440	1	MIPI1C_CAM_FRONT_CLK_P	PLACE_NEAR=U0652.AR33:3MM	7 20 53
PP9441	1	MIPI1C_CAM_FRONT_CLK_N	PLACE_NEAR=U0652.AR34:3MM	7 20 53
PP9442	1	MIPI1C_CAM_FRONT_DATA_P<0>	PLACE_NEAR=U0652.AT33:3MM	7 20 53
PP9443	1	MIPI1C_CAM_FRONT_DATA_N<0>	PLACE_NEAR=U0652.AT34:3MM	7 20 53
PP9444	1	MIPI0C_CAM_REAR_CLK_P	PLACE_NEAR=U0652.AU25:3MM	7 23 53
PP9445	1	MIPI0C_CAM_REAR_CLK_N	PLACE_NEAR=U0652.AV25:3MM	7 23 53
PP9446	1	MIPI0C_CAM_REAR_DATA_P<0>	PLACE_NEAR=U0652.AU27:3MM	7 23 53
PP9447	1	MIPI0C_CAM_REAR_DATA_N<0>	PLACE_NEAR=U0652.AV27:3MM	7 23 53

PP9450	1	PPVDD_SOC_SOC_SENSE	PLACE_NEAR=U0652.V31:1MM	
PP9451	1	PPVDD_CPU_SOC_SENSE	PLACE_NEAR=U0652.AN30:1MM	

WIFI

PP9480	1	HSIC1_WLAN2SOC_DEVICE_RDY		5 44
PP9481	1	HSIC1_WLAN2SOC_REMOTE_WAKE		5 44
PP9482	1	PMU_GPIO_WLAN_HOST_WAKE		44 48
PP9483	1	HSIC1_SOC2WLAN_HOST_RDY		5 44

GPIO_BT_WAKE	FUNC_TEST=TRUE	5 44
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FOR HSIC CHARACTERIZATION

PP9460	1	HSIC1_WLAN_DATA	PLACE_NEAR=U0652.AN33:3MM	4 44 53
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PP9462	1	HSIC1_WLAN_DATA	PLACE_NEAR=U5800.13:3MM	4 44 53
PP9463	1	HSIC1_WLAN_STB	PLACE_NEAR=U5800.14:3MM	4 44

PP9468	1	UART1_BT2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9469	1	UART1_SOC2BT_TX	PLACE_NEAR=U5800:3MM	5 44

PP9471	1	UART2_WLAN2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9472	1	UART2_SOC2WLAN_TX	PLACE_NEAR=U5800:3MM	5 44

BASEBAND

USB_BB_P	FUNC_TEST=TRUE	11 24 52
USB_BB_N	FUNC_TEST=TRUE	11 24 52

FOR HSIC CHARACTERIZATION

PP9465	1	HSIC2_BB_STB	PLACE_NEAR=U0652.B27:3MM	4 24 27
PP9466	1	HSIC2_BB_DATA	PLACE_NEAR=U3400.C7:3MM	4 24 27

PROX

HIGH SPEED, NO TEST

MIPI0C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_DATA_P<0..3>	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_DATA_N<0..3>	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23
MIPI1C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 20 53
MIPI1C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	20
MIPI1C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	20
MIPI1C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	20
MIPI1C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	20
EDP_DATA_P<0..3>	NO_TEST=TRUE	7 18
EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	7 18
EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	18

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# POWER CONNECTIONS

D

D

C

C

B

B

A

A

## BUCK0

52 46 PPVDD\_CPU == PPVDD\_CPU 9

## BUCK1

52 46 PPVDD\_GPU == PPVDD\_GPU 9

## BUCK2

52 46 PPVDD\_SOC == PPVDD\_SOC 9

## BUCK3

52 47 46 PP1V8\_S2R == PP1V8\_S2R\_MISC 5 51  
== PP1V8\_S2R\_VDDIO\_WLAN\_BT 44  
== PP1V8\_S2R\_TRISTAR 11  
== PP1V8\_S2R\_DDR 8  
== PP1V8\_S2R\_GRAPE 13  
== PP1V8\_S2R\_EXT\_SWITCH 50  
== PP1V8\_S2R\_REAR\_CAMERA  
== PP1V8\_S2R\_MESA  
== PP1V8\_S2R\_VDD\_CORE\_GPS  
== PP1V8\_S2R\_VDD\_IO\_GPS

## BUCK3\_SW

52 50 46 PP1V8\_SW1 == PP1V8\_AUDIO 15  
== PP1V8\_DMIC 14  
== PP1V8\_CAM\_FRONT 20  
== PP1V8\_CAM\_REAR 23  
== PP1V8\_PROX 22

52 50 46 PP1V8\_EXT\_SW == PP1V8\_VDDIO18\_SOC 8 9  
== PP1V8\_SOC 4 5 7 10 18  
== PP1V8\_MIPI\_SOC 7  
== PP1V8\_EDP\_SOC 7  
== PP1V8\_NAND\_SOC 6  
== PP1V8\_NAND 12 48  
== PP1V8\_PLL\_SOC 4  
== PP1V8\_SPKRAMP  
== PP1V8\_EEPROM 51  
== PP1V8\_BEACON

52 46 PP1V8\_SW2 == PP1V8\_GRAPE 13

46 PP1V8\_S2R\_SW3 == PP1V8\_S2R\_GYRO 21  
== PP1V8\_S2R\_ACCEL 21  
== PP1V8\_S2R OSCAR 19  
PP1V8\_S2R\_SW3 COMP 52 54

54 52 PP1V8\_S2R\_SW3\_COMP == PP1V8\_S2R\_COMP 21

PP1V8\_S2R\_SW3 SHOULD BE ON IN HIBERNATE  
CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

## BUCK4

52 47 46 PP1V2\_S2R == PP1V2\_S2R\_DDR 8  
== PP1V2\_S2R\_DDR\_SOC 8  
== PP1V2\_S2R\_CAM\_REAR

## BUCK4\_SW

52 46 PP1V2\_SW1 == PP1V2\_VDDO\_DDR 8  
== PP1V2\_VDDIOD\_SOC 8  
== PP1V2\_HSIC\_SOC 4

52 46 PP1V2\_S2R\_SW2 == PP1V2\_S2R OSCAR 19  
PP1V2\_S2R\_SW2 SHOULD BE ON IN HIBERNATE  
PROVIDE 1.2V TO OSCAR

## BUCK5

52 46 PPVDD\_SRAM == PPVDD\_SRAM\_CPU  
== PPVDD\_SRAM\_SOC 9

## BUCK6

52 46 PP3V3\_S2R == PP3V3\_S2R\_SWITCH 48  
== PP3V3\_S2R\_WIFI\_PA 44

52 48 PP3V3\_SW == PP3V3\_EDP\_PU  
== PP3V3\_NAND 12  
== PP3V3\_USB\_SOC 4

## LDO1

52 47 PP3V0\_SPARE1 == PP3V0\_SPARE1 49

## LDO2

52 47 16 PP1V7\_VA\_VCP == PP1V7\_VA\_VCP 15 16

## LDO3

LDO3 SHOULD BE ON IN HIBERNATE  
COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR  
HALL EFFECT NEEDS TO BE ON IN HIBERNATE

52 47 PP3V0\_S2R\_SENSOR == PP3V0\_S2R\_HALL 13  
== PP3V0\_S2R\_GYRO 21  
== PP3V0\_S2R\_ACCEL 21  
== PP3V0\_S2R\_COMP 21

## LDO4

52 47 PP3V0\_ALS == PP3V0\_ALS 20  
== PP3V0\_PROX 22  
== PP3V0\_HP\_ALS  
== PP3V0\_IO\_ALS  
SHOULD IO ALS POWER HERE?

## LDO5

52 47 PP3V0\_UVLO == PP3V0\_UVLO 49

## LDO6

52 47 PP3V3\_ACC == PP3V3\_ACC 11

## LDO7

LDO7 SHOULD BE ON IN HIBERNATE

52 47 PP3V0\_S2R\_TRISTAR == PP3V0\_S2R\_TRISTAR 11

## LDO8

47 NC\_LDO8 NO\_TEST=TRUE == NC\_LDO8

## LDO9

BACKUP RAIL. CAN BE BOOSTED TO MEET  
1.1V MIN ON CAMERA IF NEEDED.

52 47 PP1V3\_CAM == PP1V3\_CAM\_FRONT  
== PP1V3\_CAM\_REAR 23

## LDO10

52 47 PP1V0\_SOC == PP1V0\_USB\_SOC 4  
== PP1V0\_MIPI\_SOC 7  
== PP1V0\_EDP\_PAD\_DVDD\_SOC 7

## LDO11

52 47 PP2V6\_CAM\_AF == PP2V6\_CAM\_REAR\_AF 23

## LDO13

52 47 PP2V9\_CAM == PP2V9\_CAM\_FRONT 20  
== PP2V9\_CAM\_REAR 23

## VLCDM1

47 PP5V25\_GRAPE == PP5V25\_GRAPE 13

## CHARGER MAIN

52 49 48 47 46 PPVCC\_MAIN == PPVCC\_MAIN\_AUDIO 15 16  
== PPVCC\_MAIN\_LED 47  
== PPVCC\_MAIN\_DOCK 43  
== PPVCC\_MAIN\_DEV  
== PPVCC\_MAIN\_CPU 46  
== PPVCC\_MAIN\_GPU 46  
== PPVCC\_MAIN\_SOC 46  
== PPVCC\_MAIN\_GRAPE 13  
== PPVCC\_MAIN\_LCD 18  
== PPVCC\_MAIN\_NAVAJO 47  
== PPVCC\_MAIN\_VDD\_LCM 44  
== PPVCC\_MAIN\_WLAN  
== PPVCC\_MAIN\_GPS

## BATTERY

52 46 PPBATT\_VCC == PPBATT\_POS\_CONN 45  
== PPBATT\_VCC\_BB 24 25 33 34 35 36 37 38  
== PPBATT\_AUDIO

## USB POWER INPUT

52 46 PPVBUS\_USB\_DCIN == PPVBUS\_USB\_EMI 43

## ON\_BUF

52 47 PP1V8\_ALWAYS == PP1V8\_ALWAYS 5

## BACKLIGHT BOOST

52 47 PPLED\_OUT\_A == PPLED\_REG\_A 18

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